FIG. 1

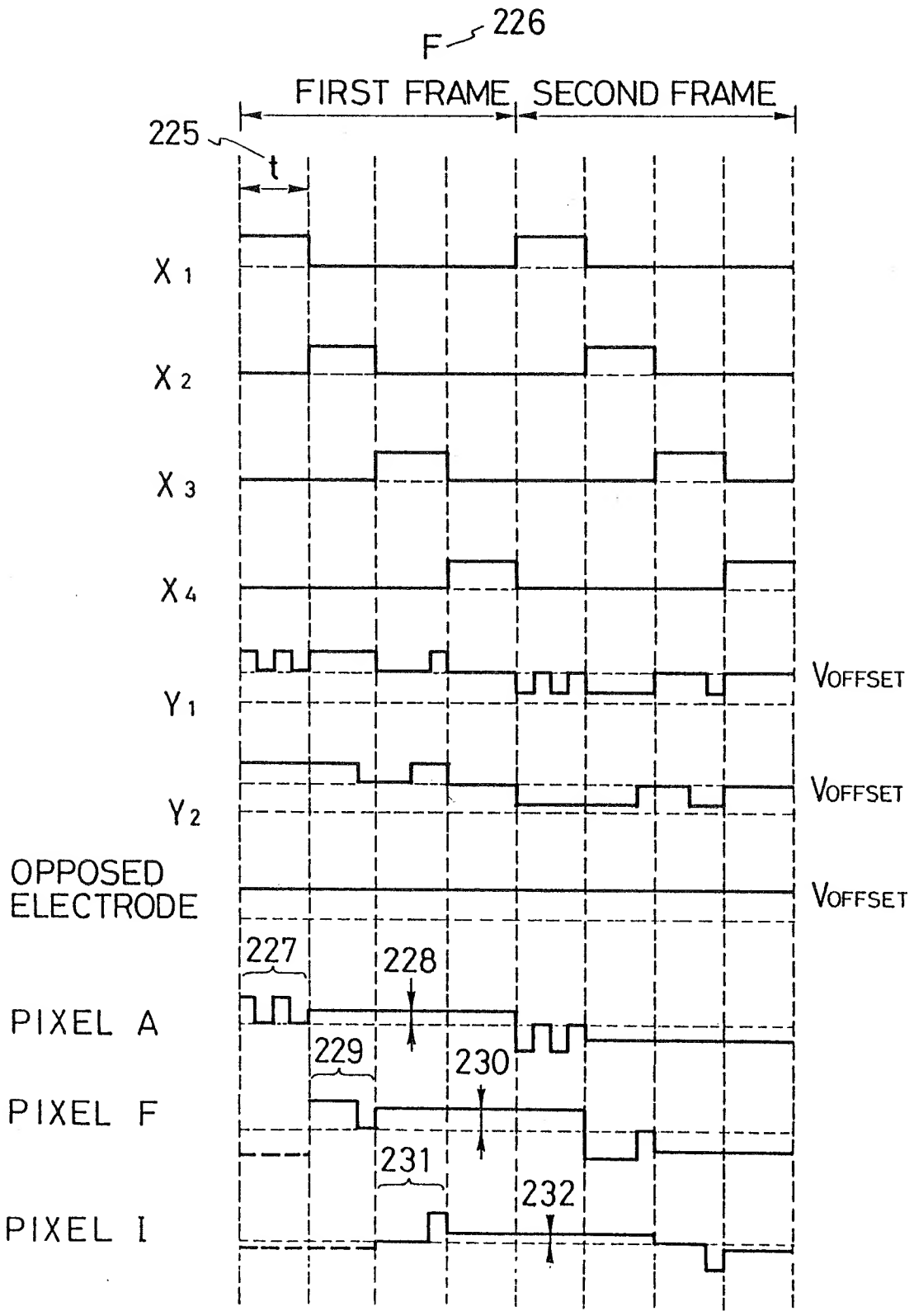

F
226
FIRST FRAME
SECOND FRAME
225
t
X 1
X 2
X 3
X 4
Y 1
Y 2
OPPOSED ELECTRODE
VOFFSET
VOFFSET
VOFFSET
227
228
229
230
231
232
PIXEL A
PIXEL F
PIXEL I

FIG. 2

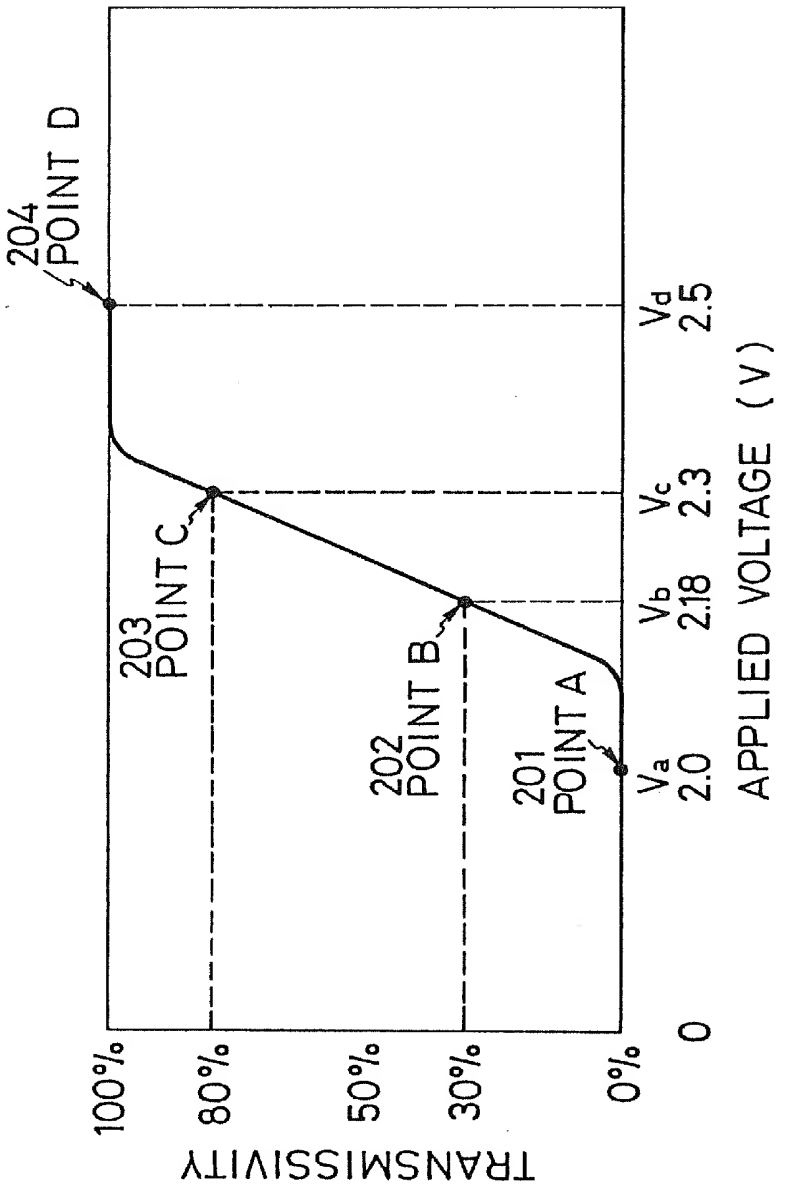
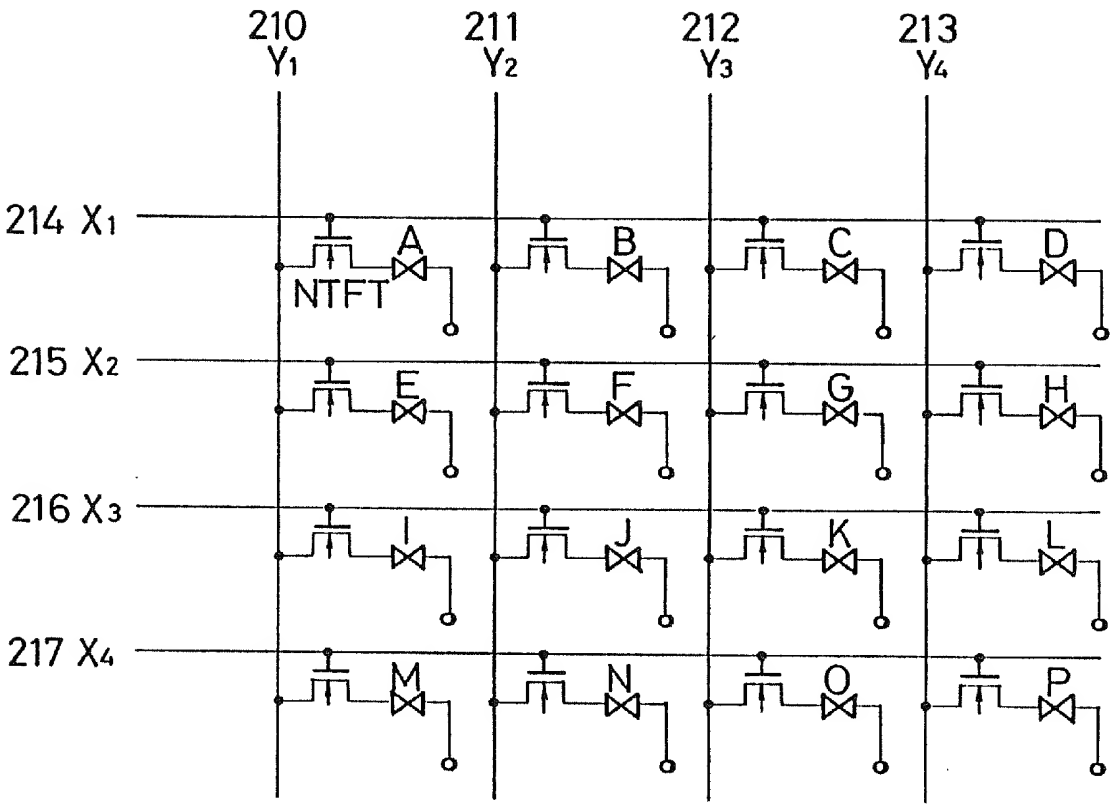

204
POINT D
203
POINT C
202
POINT B
201
POINT A
100%
80%
50%
30%
0%
TRANSMISSIVITY
0
V_a 2.0
V_b 2.18
V_c 2.3
V_d 2.5
APPLIED VOLTAGE (V)

FIG. 3


210
Y1
211
Y2
212
Y3
213
Y4
214 X1
215 X2
216 X3
217 X4
A
NTFT
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P

PRIOR ART

FIG. 4

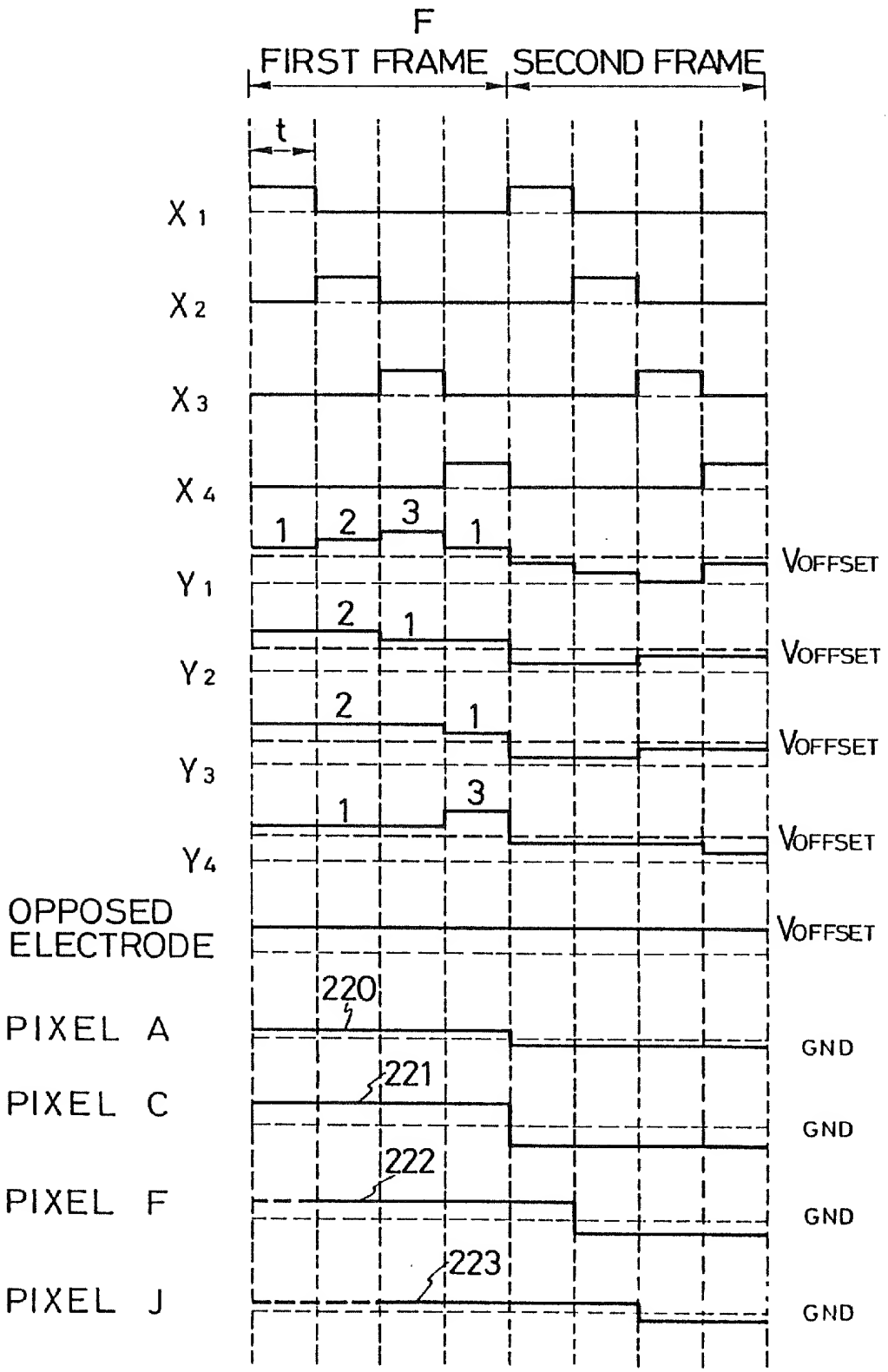


FIG. 5

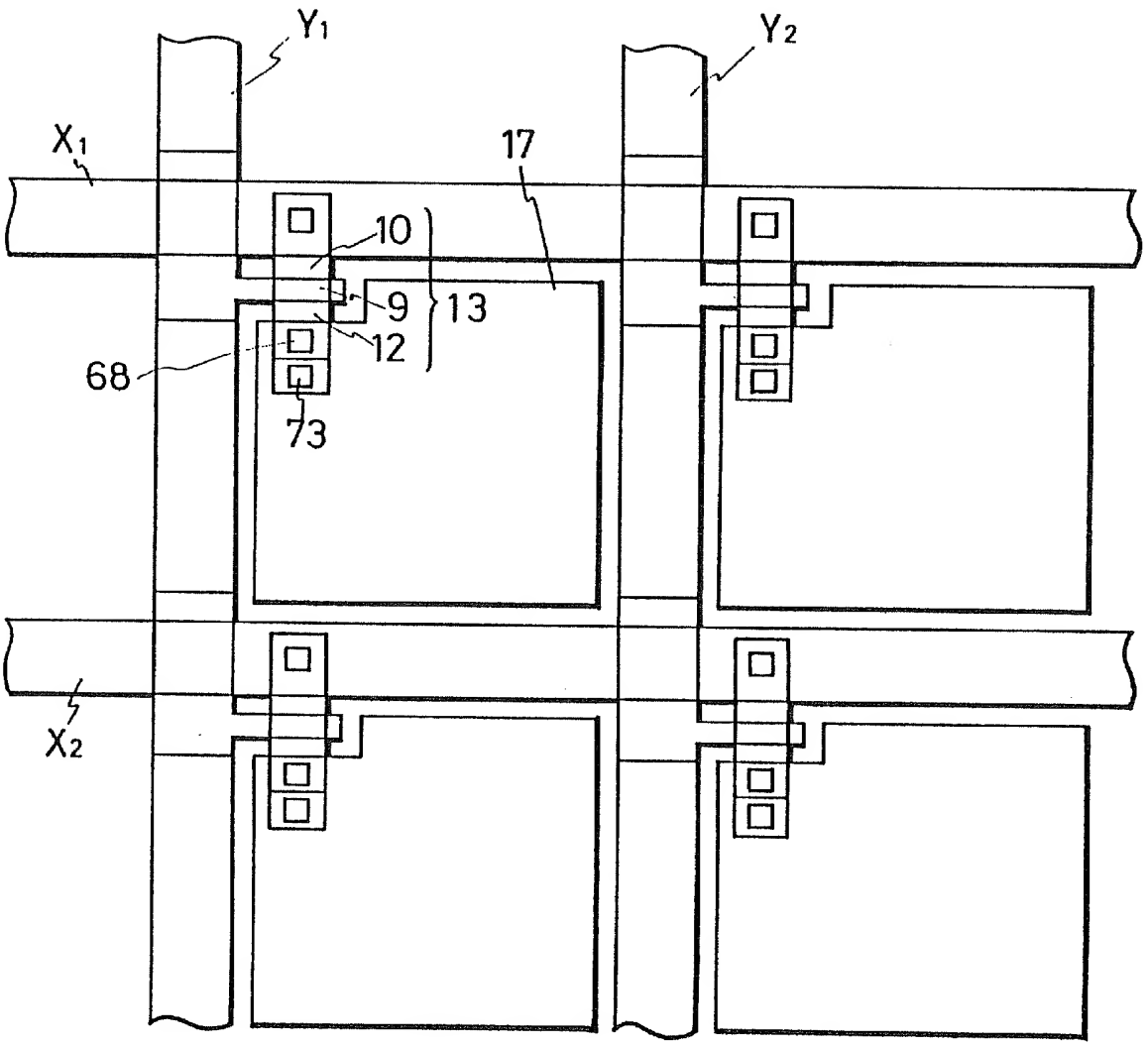


FIG. 6(A)

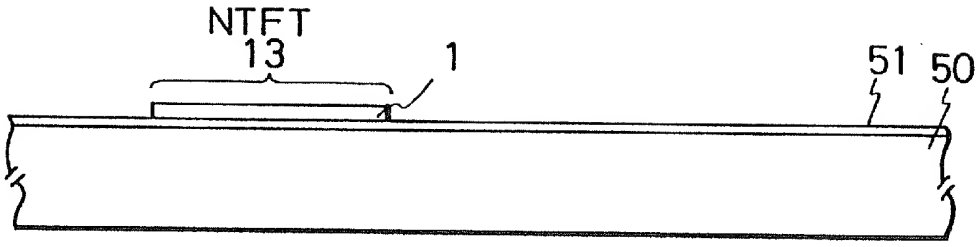


FIG. 6(B)

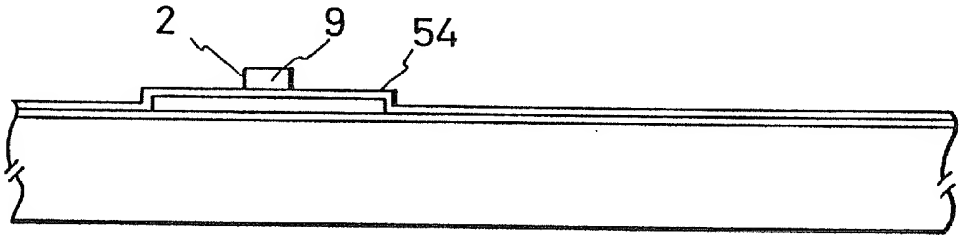


FIG. 6(C)

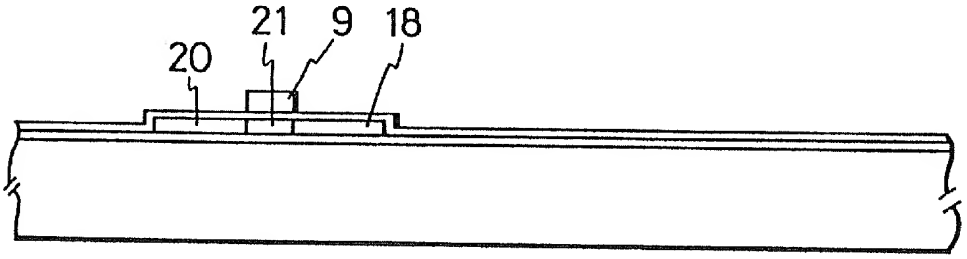


FIG. 6(D)

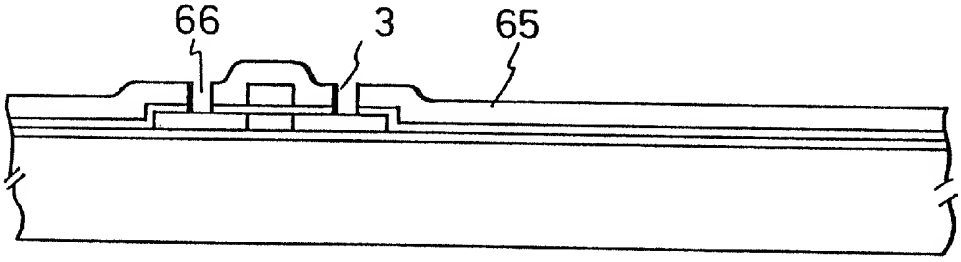


FIG. 6(E)

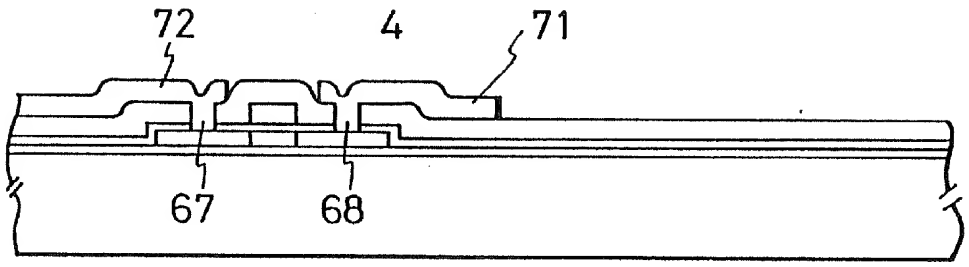


FIG. 6(F)

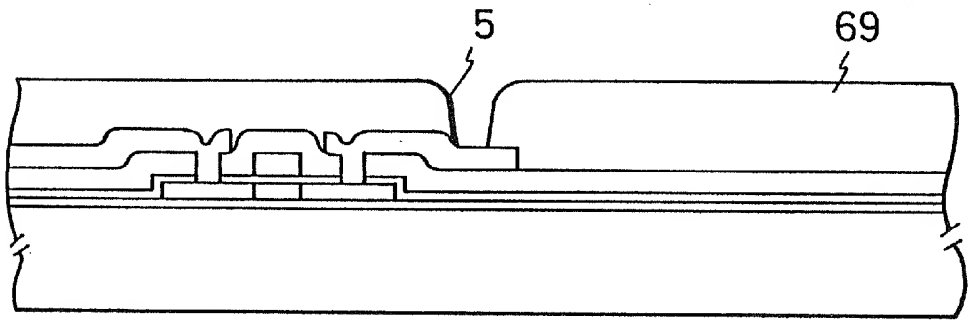


FIG. 6(G)

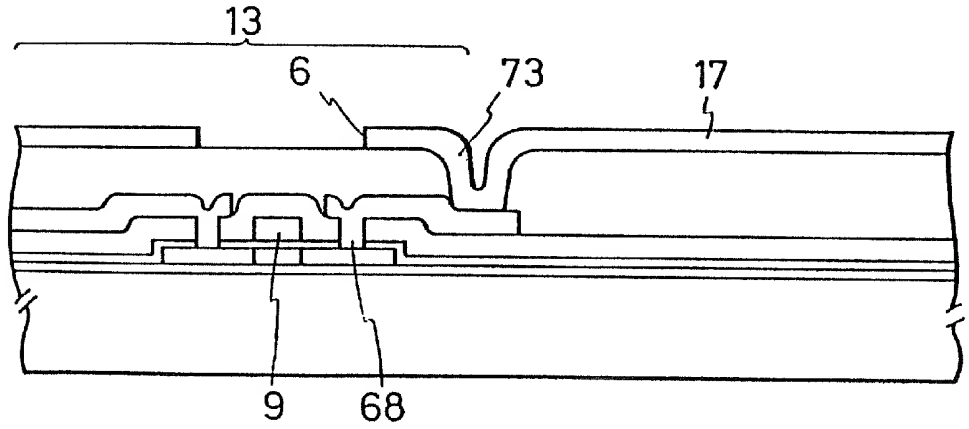


FIG. 7

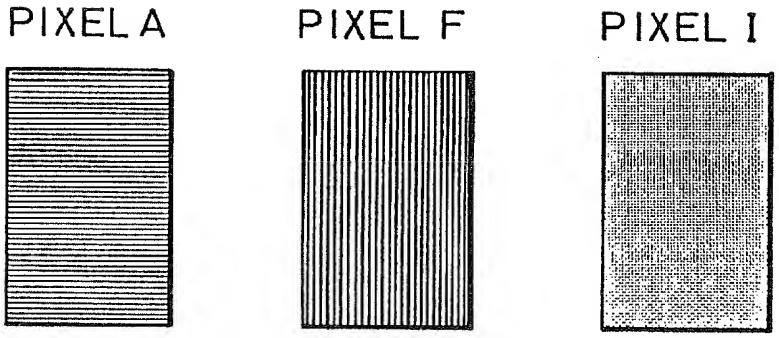


FIG. 8

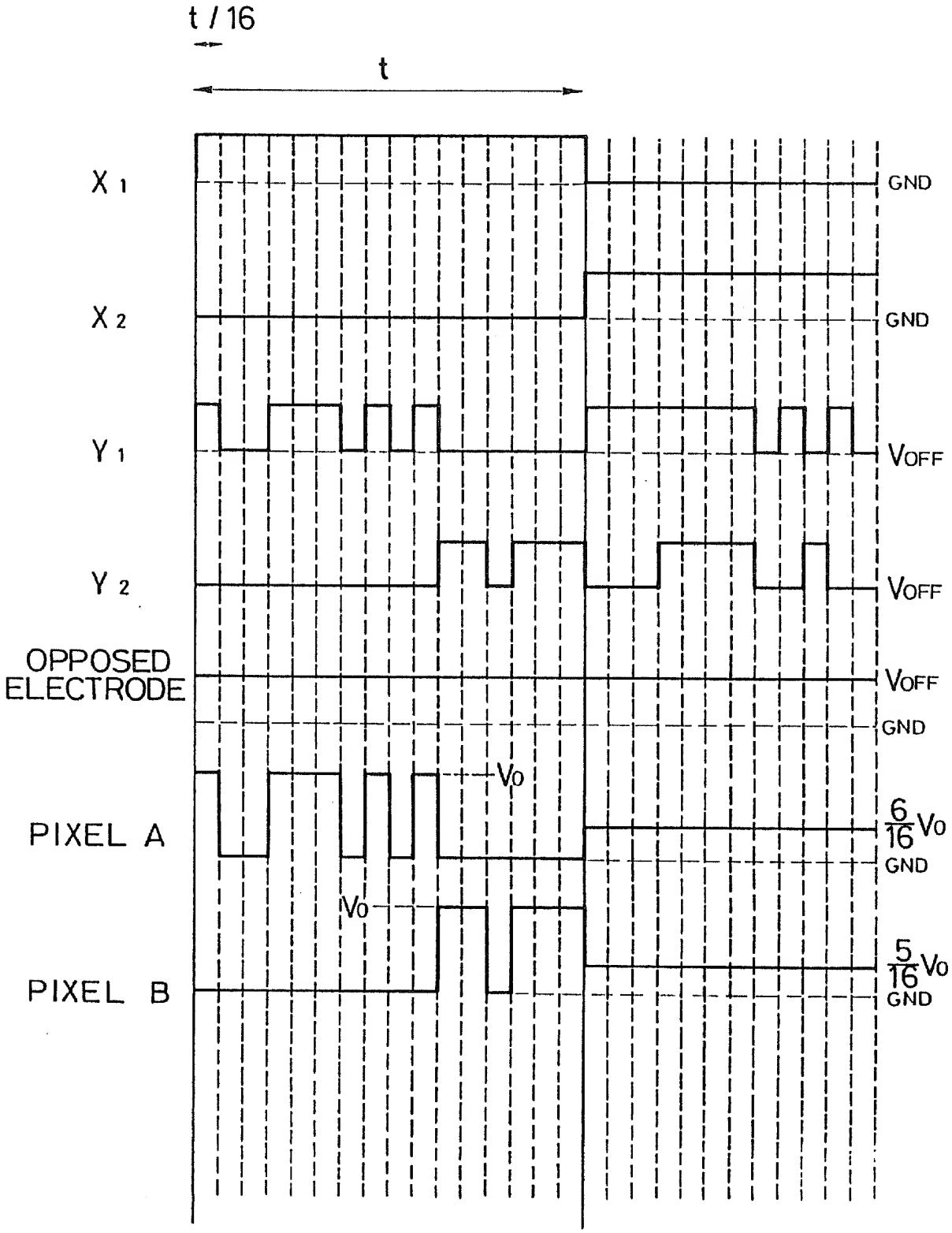

t / 16
t
X 1
X 2
Y 1
Y 2
OPPOSED ELECTRODE
PIXEL A
PIXEL B
GND
GND
VOFF
VOFF
VOFF
GND
Vo
Vo
6/16 Vo
GND
5/16 Vo
GND

FIG. 9

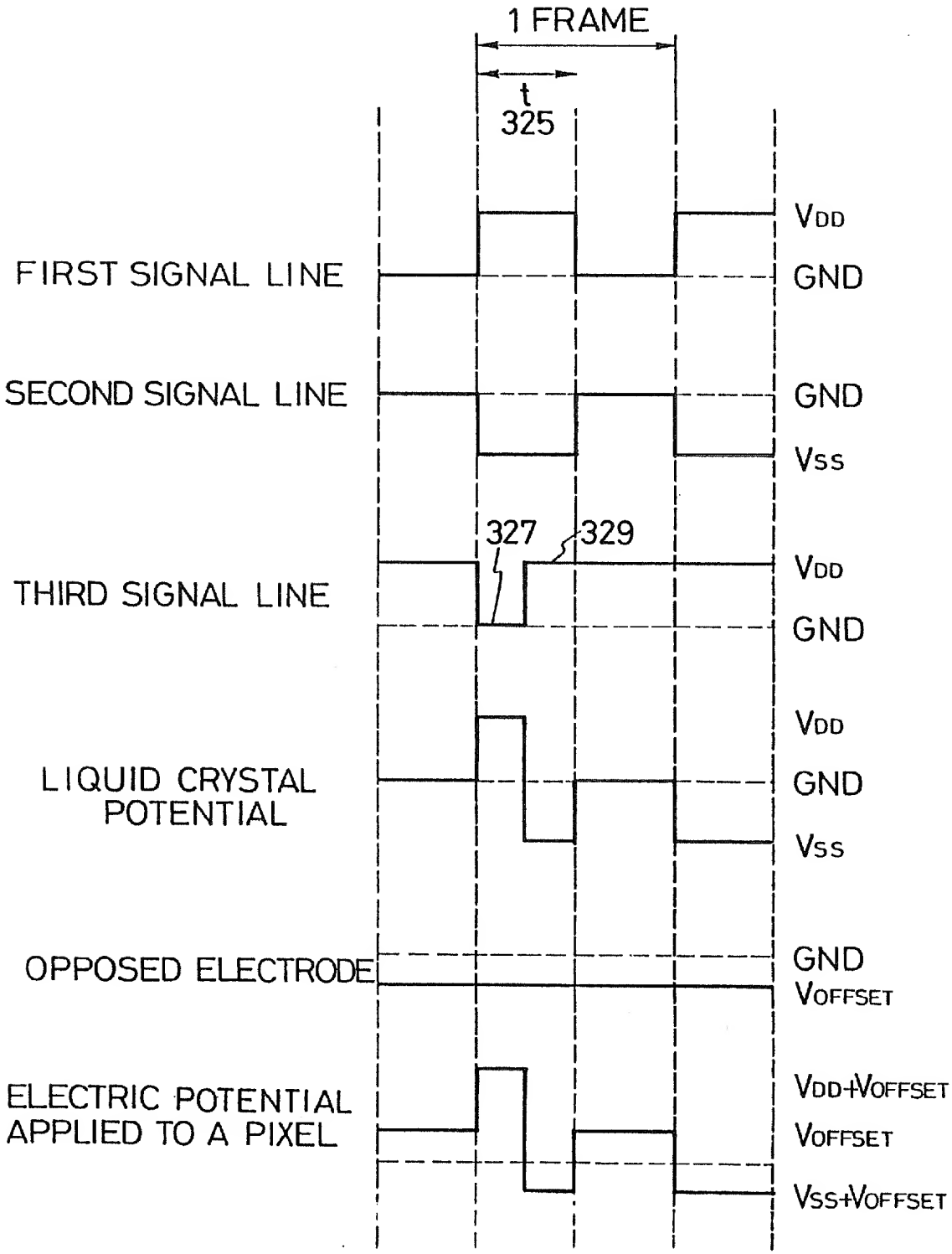
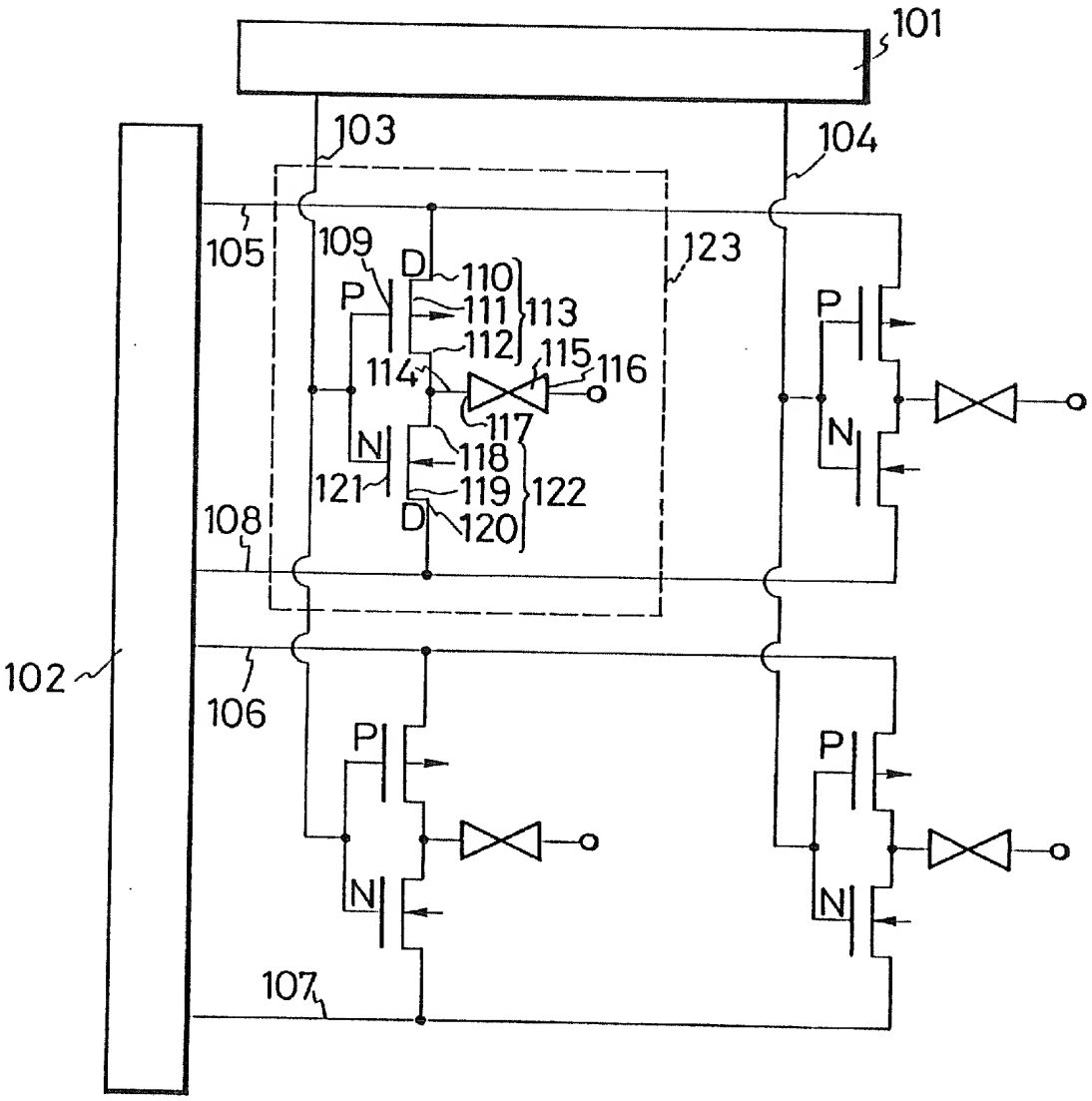

1 FRAME
t
325
FIRST SIGNAL LINE
SECOND SIGNAL LINE
THIRD SIGNAL LINE
LIQUID CRYSTAL POTENTIAL
OPPOSED ELECTRODE
ELECTRIC POTENTIAL APPLIED TO A PIXEL
327
329
VDD
GND
Vss
VOFFSET
VDD+VOFFSET
Vss+VOFFSET

FIG. 10


101
103
104
105
109
D
110
P
111
113
112
123
P
114
115
116
117
N
118
N
121
119
122
108
D
120
102
106
P
P
N
N
107

PRIOR ART

FIG. 11

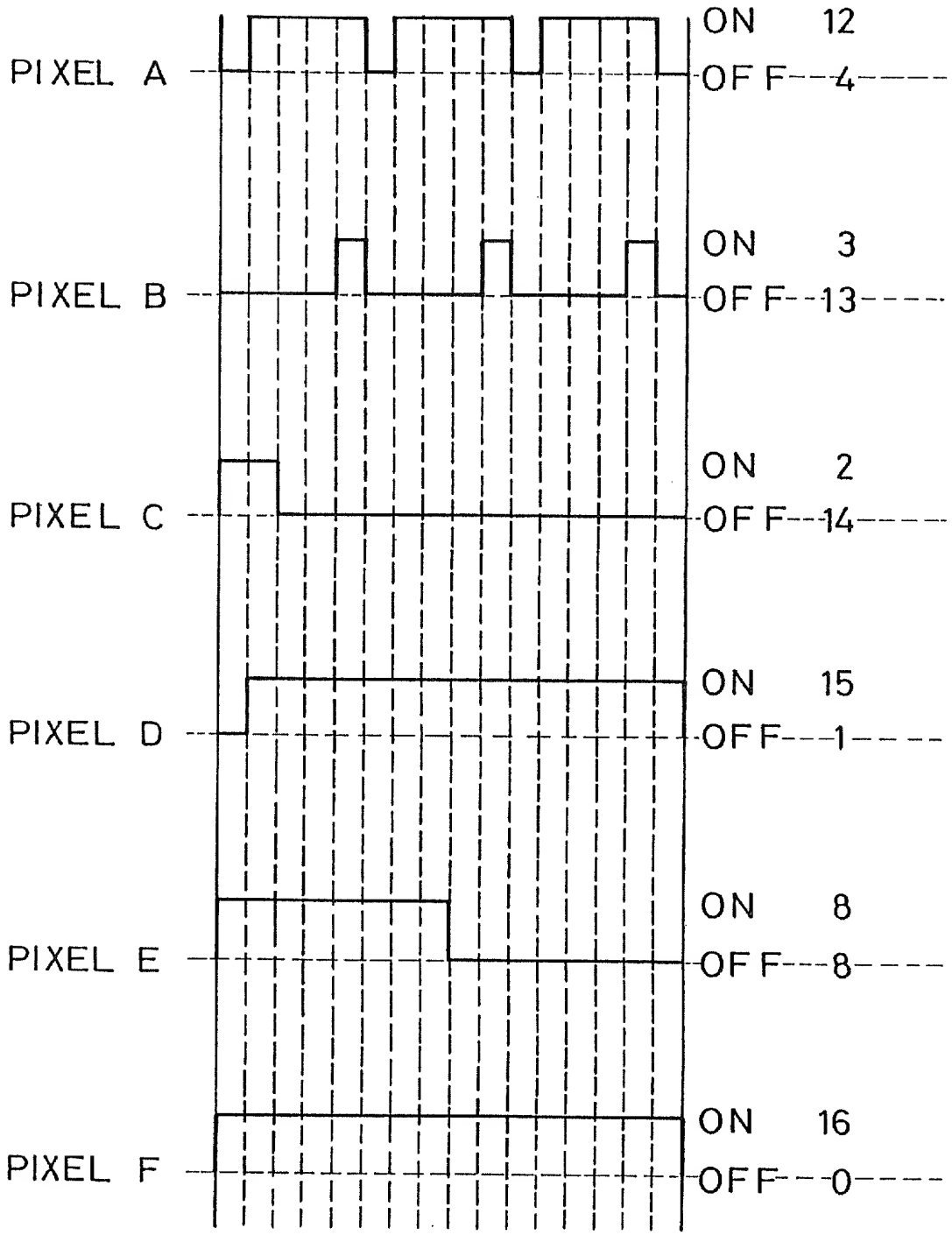


FIG. 12

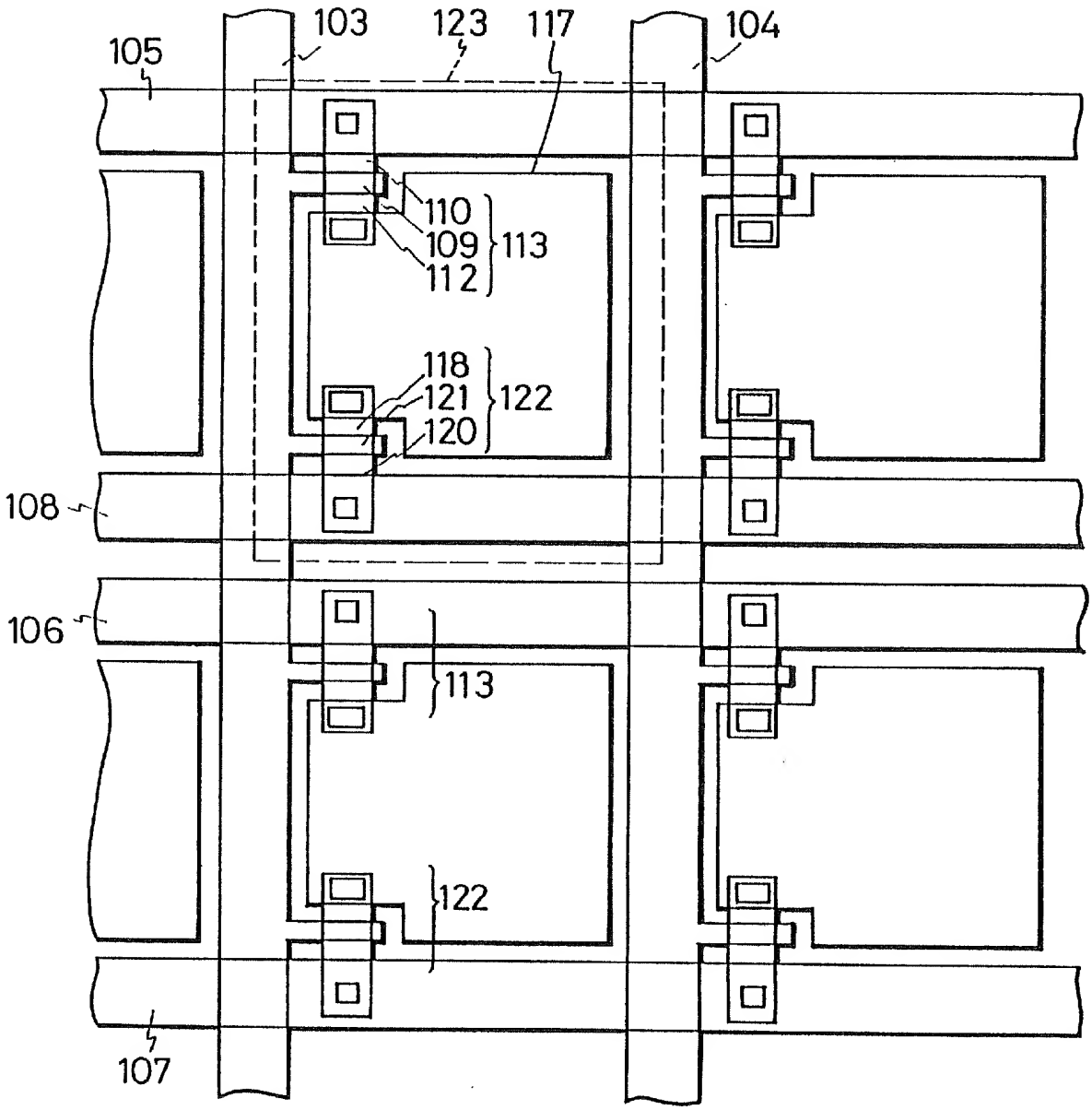

103
123
117
104
105
110
109
112
113
118
121
120
122
108
106
113
122
107

FIG. 13(A)

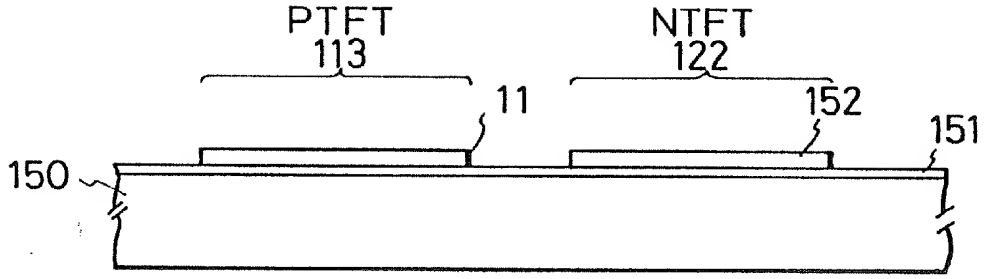


FIG. 13(B)

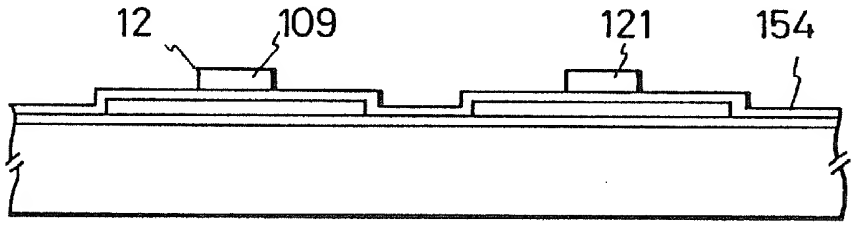


FIG. 13(C)

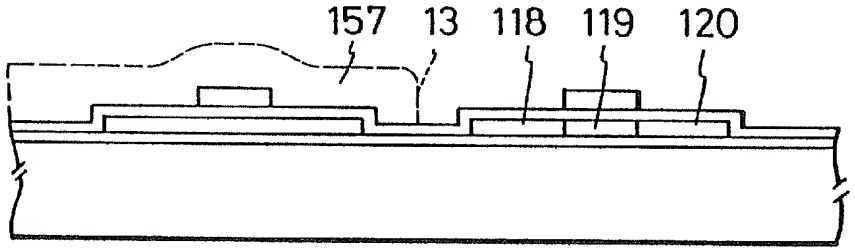


FIG. 13(D)

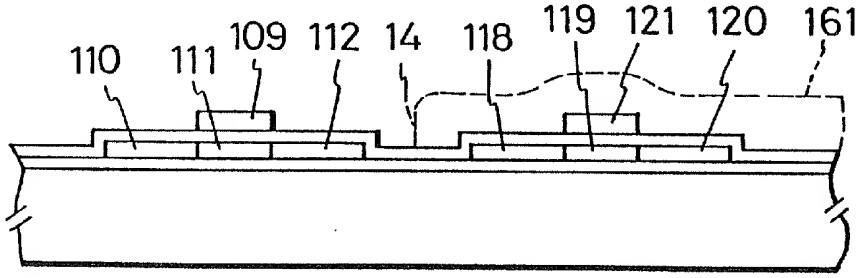


FIG. 13(E)

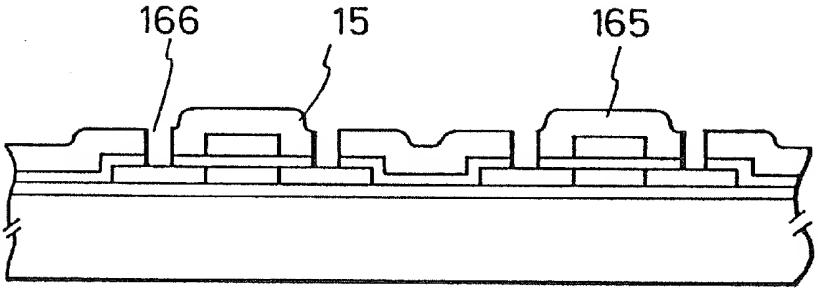


FIG. 13(F)

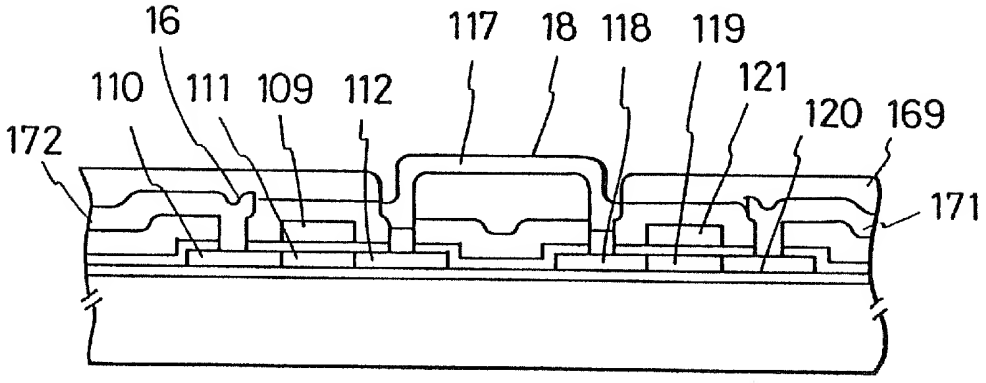


FIG. 14

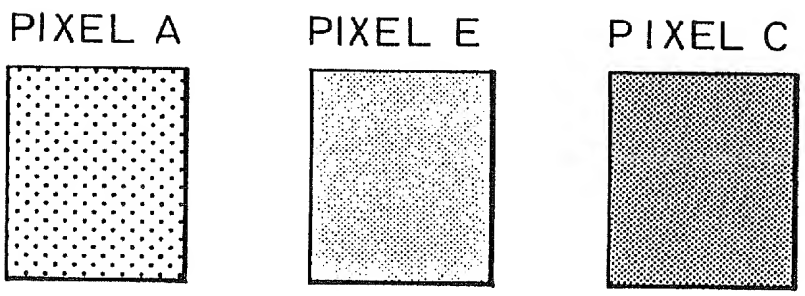


FIG. 15

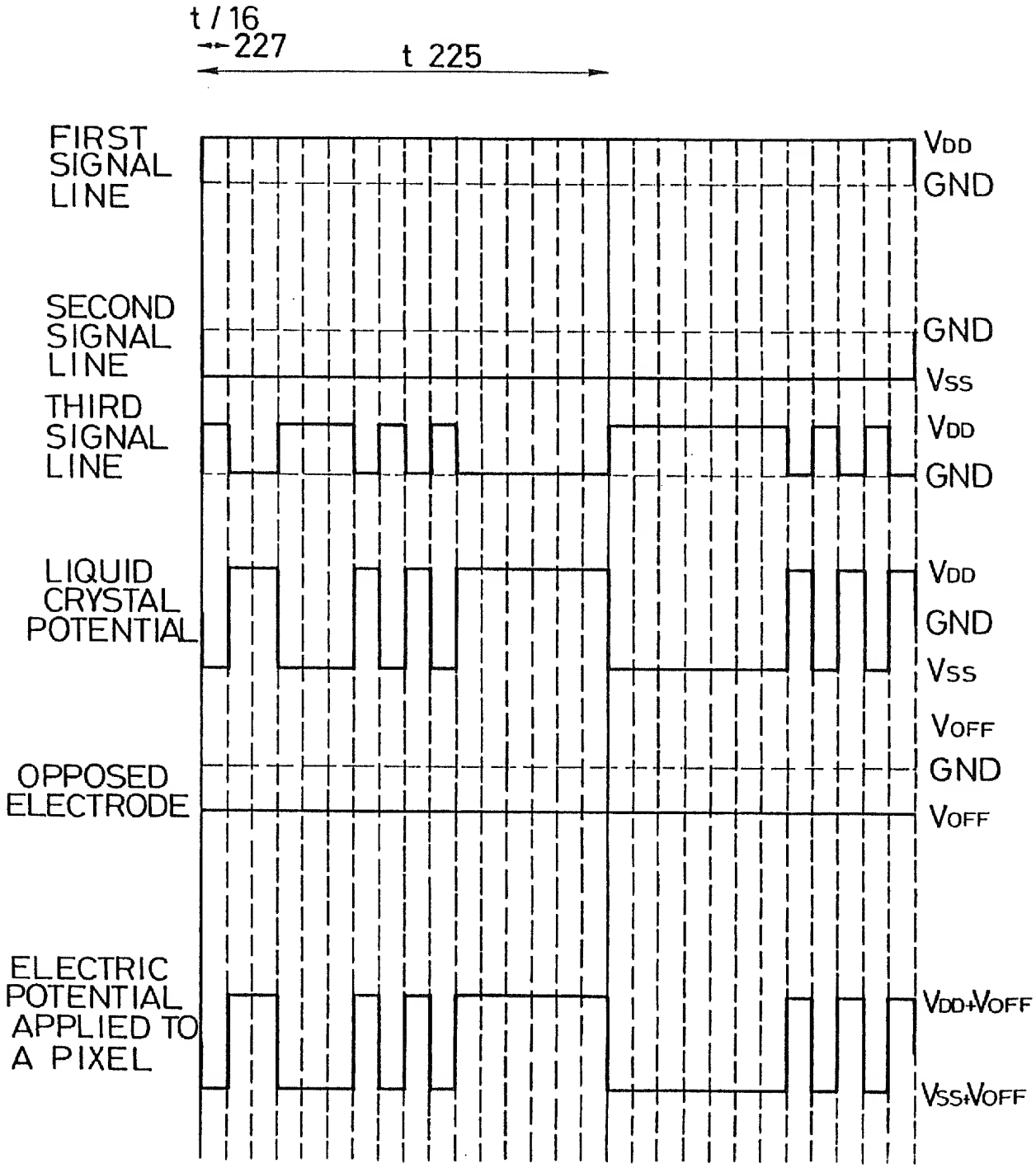

t / 16
227
t 225
FIRST SIGNAL LINE
SECOND SIGNAL LINE
THIRD SIGNAL LINE
LIQUID CRYSTAL POTENTIAL
OPPOSED ELECTRODE
ELECTRIC POTENTIAL APPLIED TO A PIXEL
VDD
GND
GND
VSS
VDD
GND
VDD
GND
VSS
VOFF
GND
VOFF
VDD+VOFF
VSS+VOFF

FIG. 16

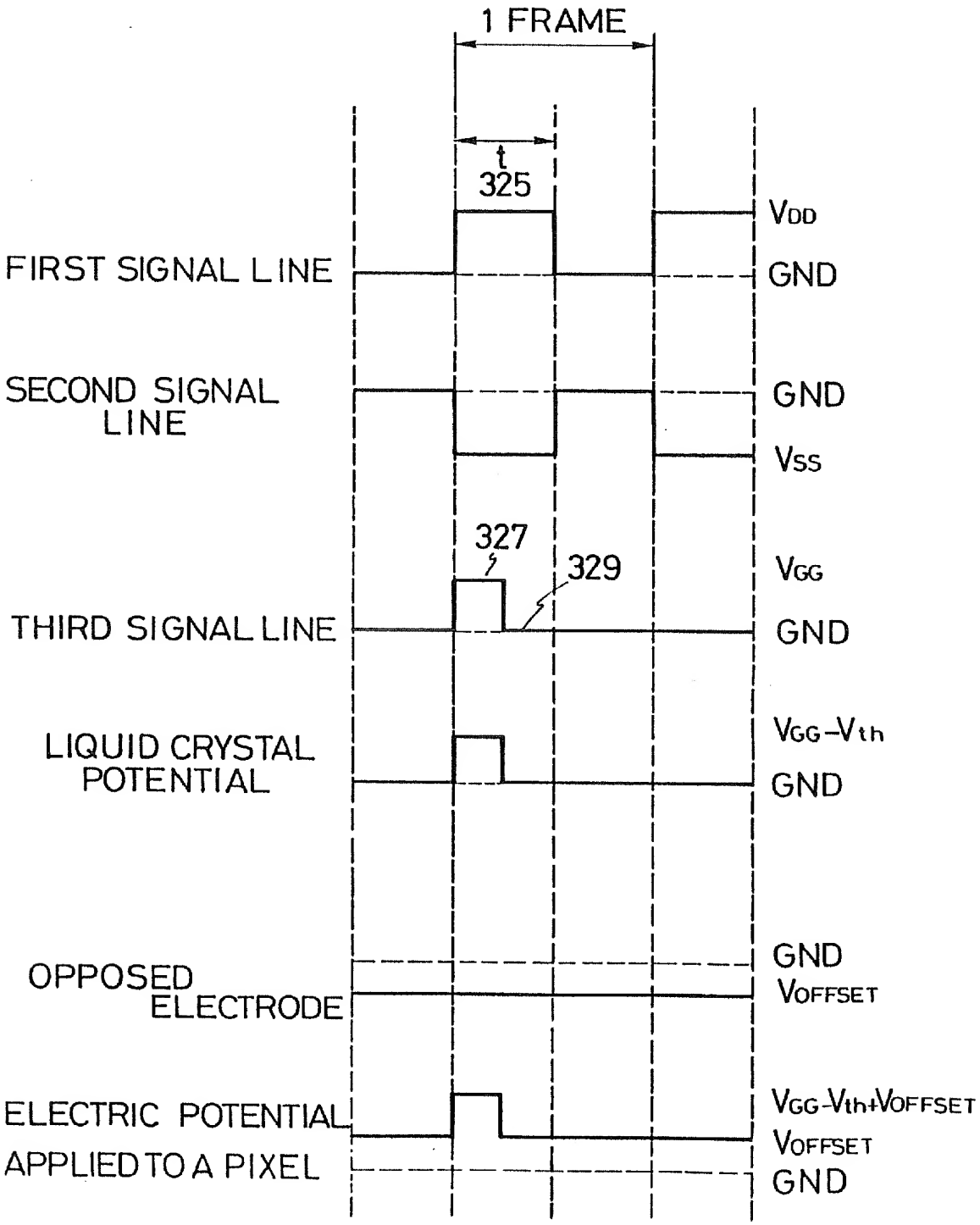

1 FRAME
t
325
FIRST SIGNAL LINE
VDD
GND
SECOND SIGNAL LINE
GND
VSS
327
329
THIRD SIGNAL LINE
VGG
GND
LIQUID CRYSTAL POTENTIAL
VGG-Vth
GND
OPPOSED ELECTRODE
GND
VOFFSET
ELECTRIC POTENTIAL APPLIED TO A PIXEL
VGG-Vth+VOFFSET
VOFFSET
GND

FIG. 17

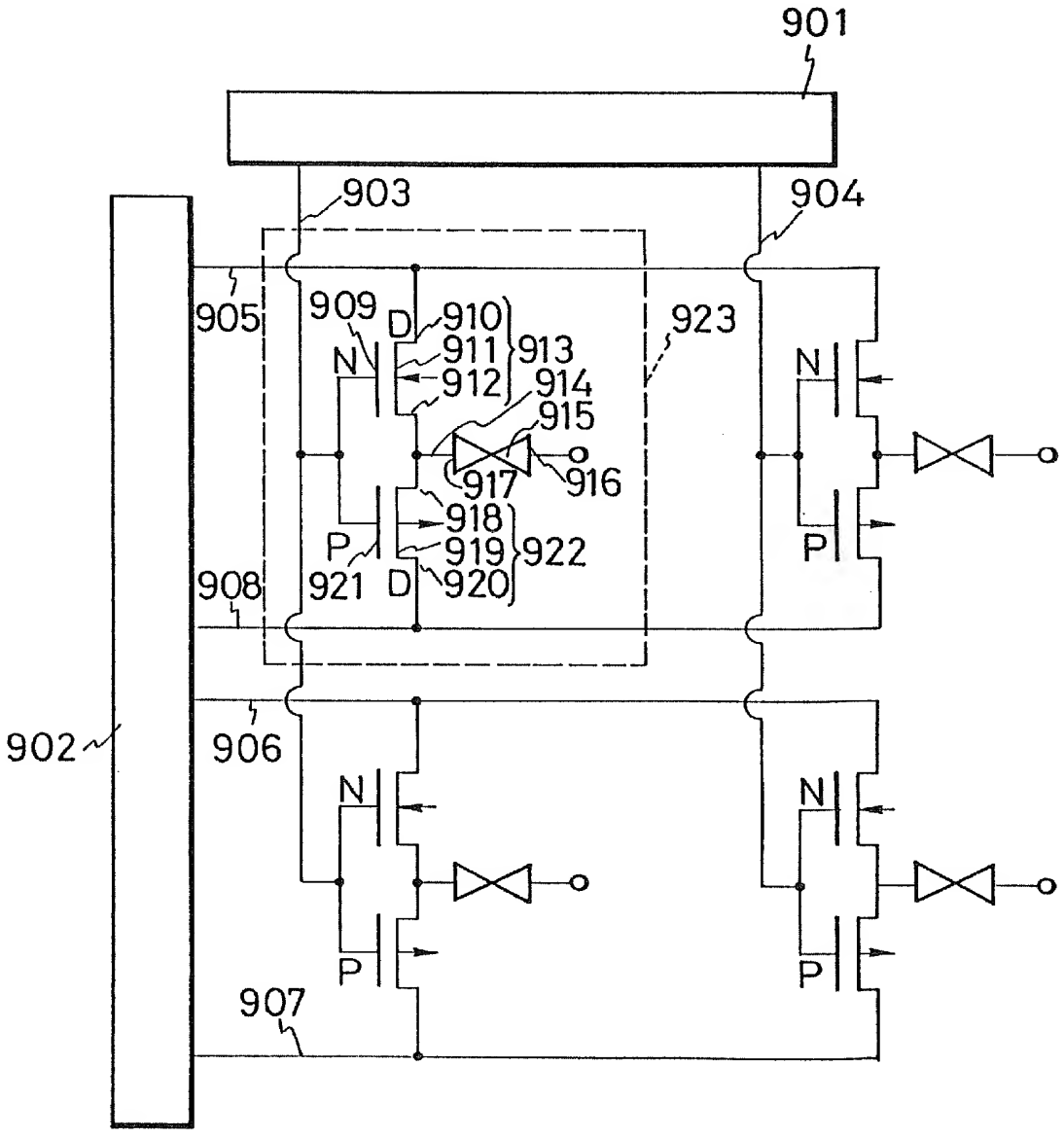

901
903
904
905
909
D
910
911
912
913
923
N
914
915
916
917
918
919
920
921
922
P
908
906
902
907

FIG. 18(A)

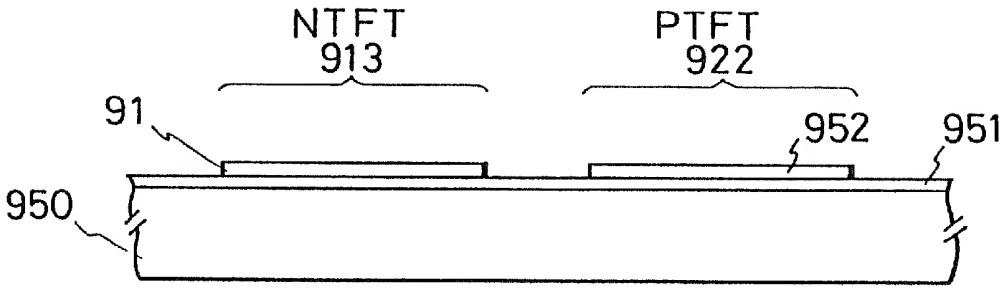


FIG. 18(B)

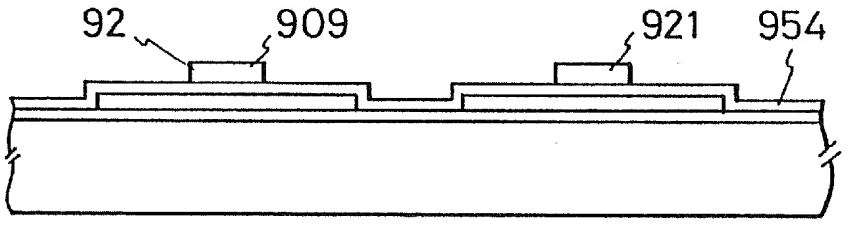


FIG. 18(C)

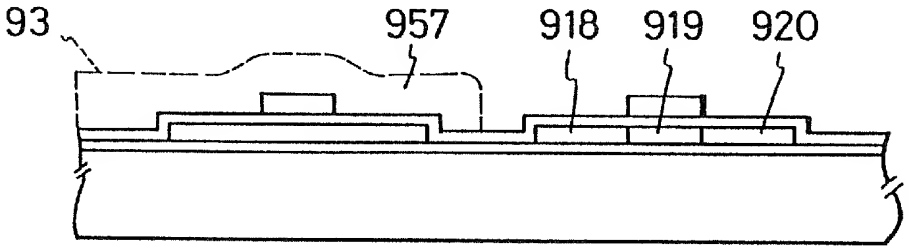


FIG. 18(D)

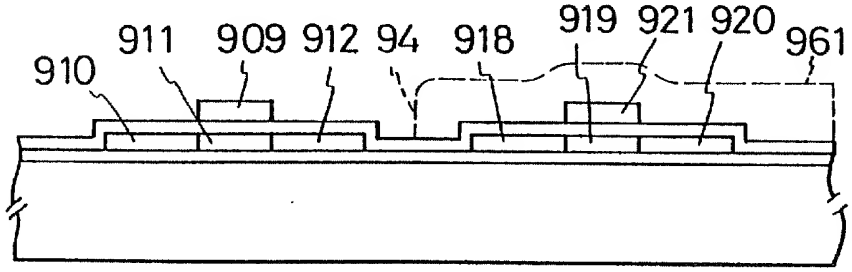


FIG. 18(E)

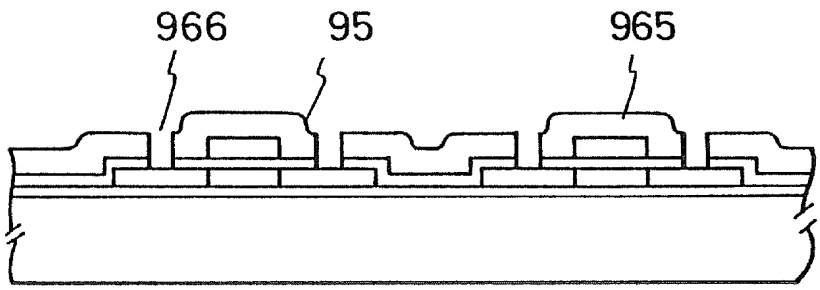


FIG. 18(F)

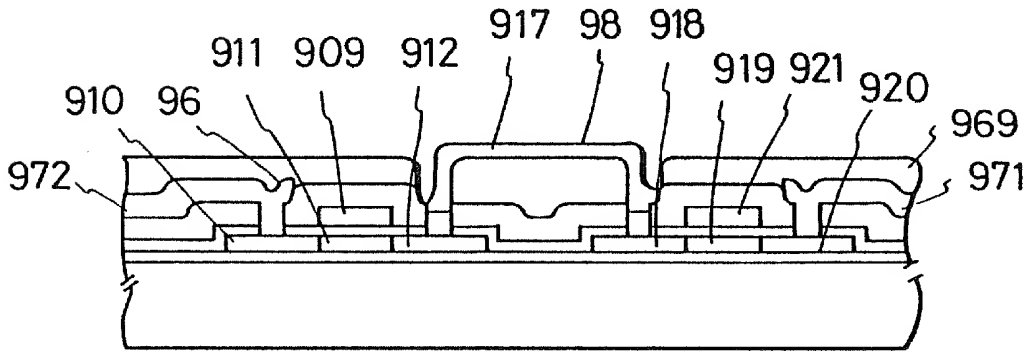


FIG. 19

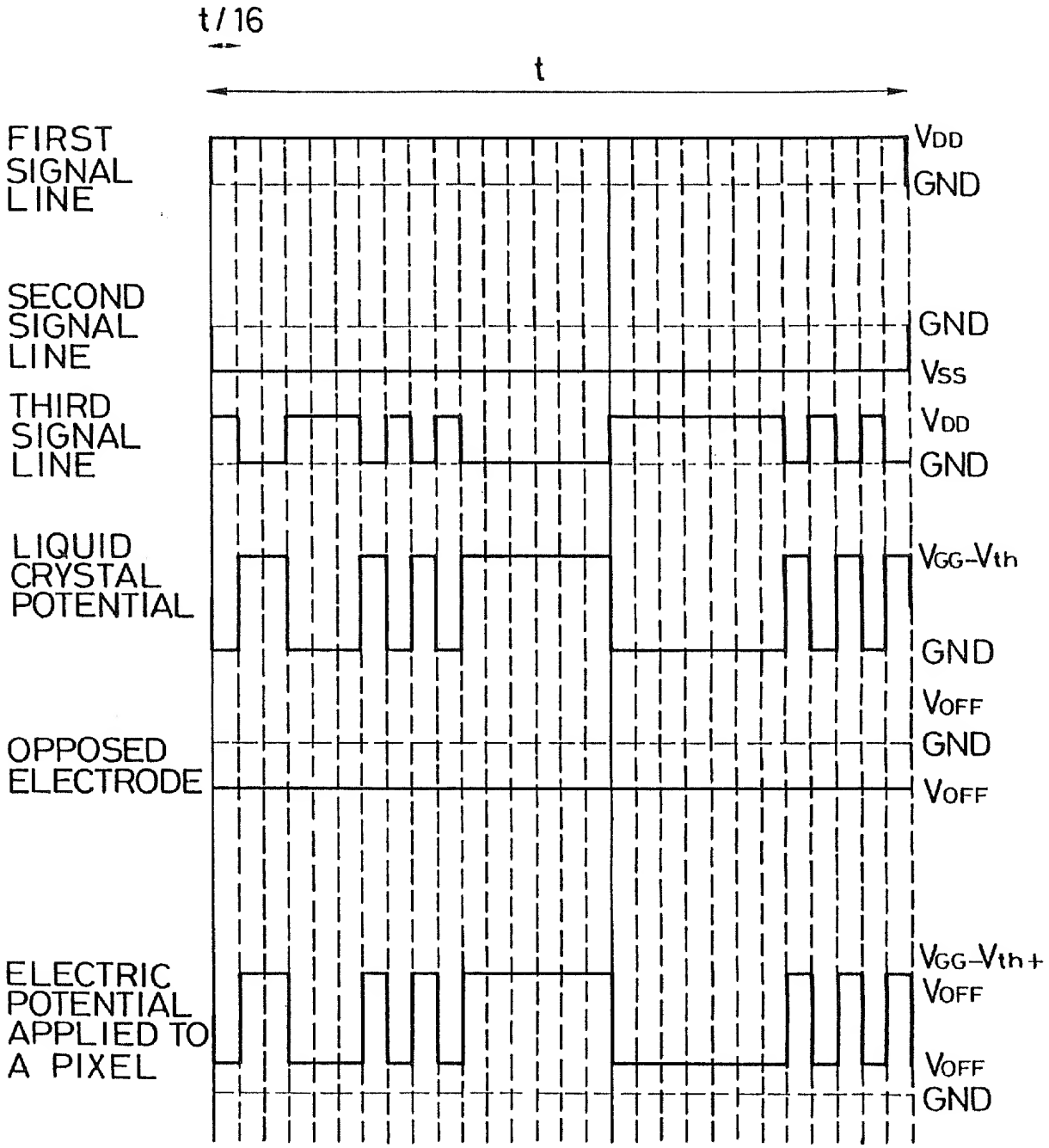

t/16
t
FIRST SIGNAL LINE
SECOND SIGNAL LINE
THIRD SIGNAL LINE
LIQUID CRYSTAL POTENTIAL
OPPOSED ELECTRODE
ELECTRIC POTENTIAL APPLIED TO A PIXEL
VDD
GND
GND
VSS
VDD
GND
VGG-Vth
GND
VOFF
GND
VOFF
VGG-Vth+
VOFF
VOFF
GND

FIG. 20

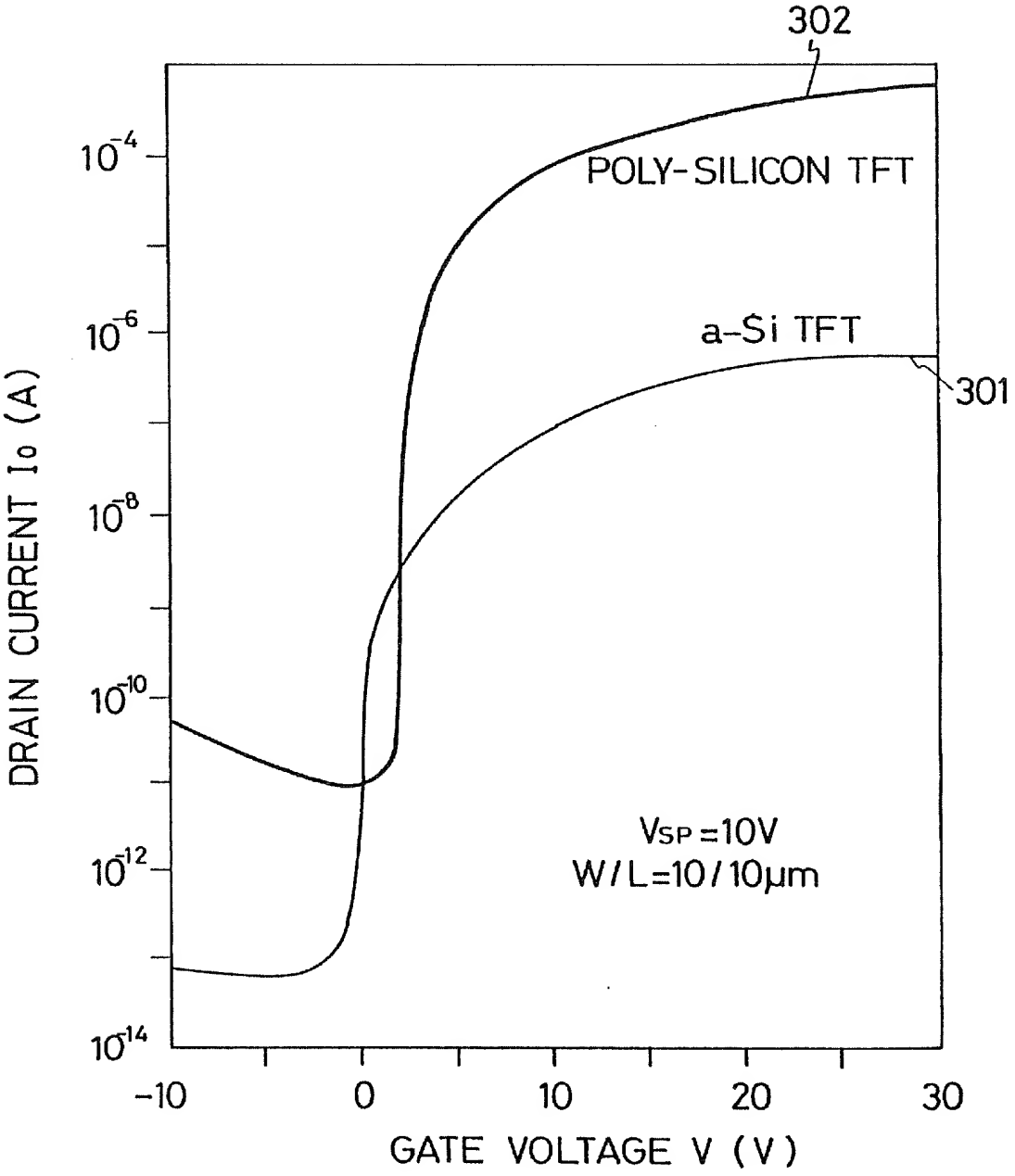

302
POLY-SILICON TFT
a-Si TFT
301
10^{-4}
10^{-6}
10^{-8}
10^{-10}
10^{-12}
10^{-14}
DRAIN CURRENT I_D (A)
V_{SP} =10V
W/L=10/10μm
-10
0
10
20
30
GATE VOLTAGE V (V)

FIG. 21

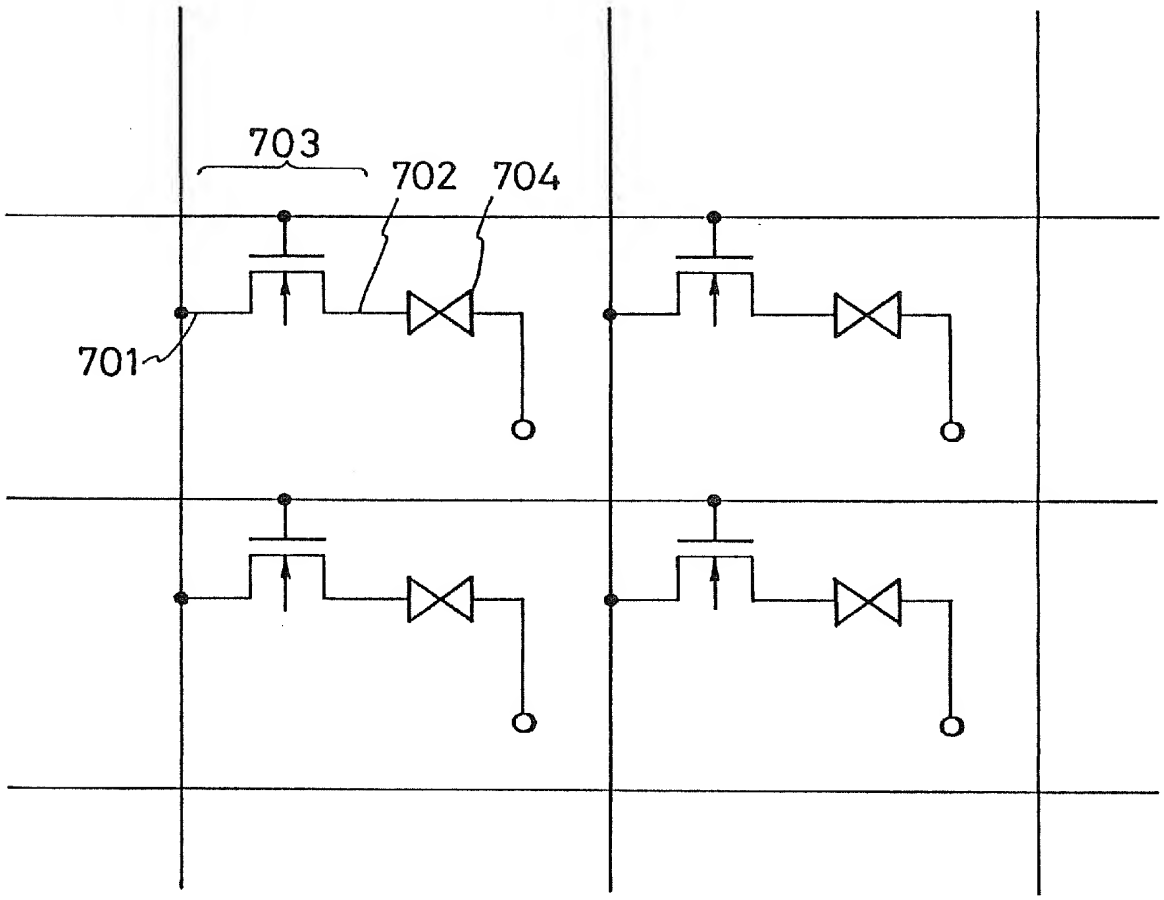


FIG. 22(A)

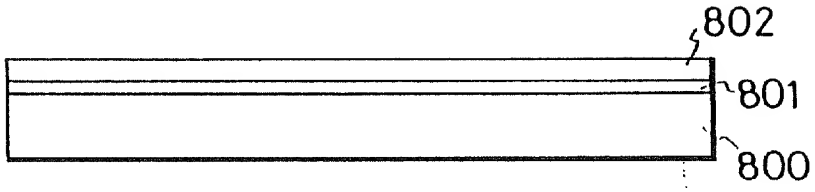


FIG. 22(B)

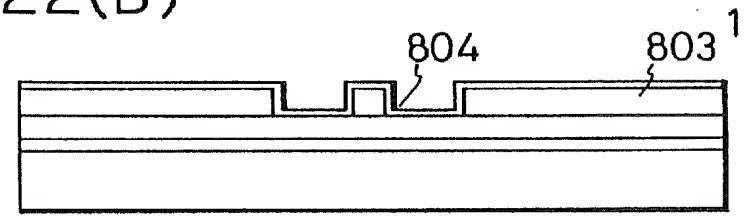


FIG. 22(C)

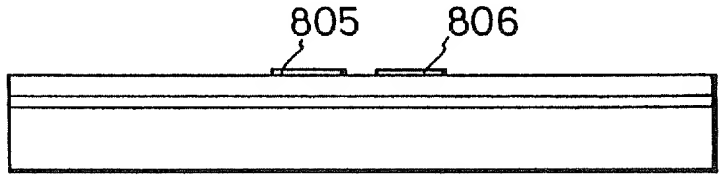


FIG. 22(D)

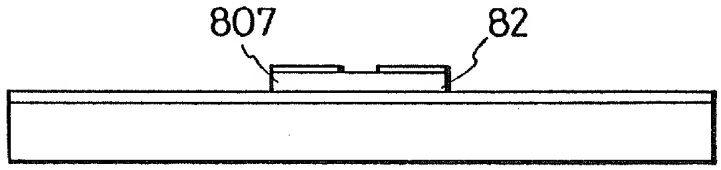


FIG. 22(E)

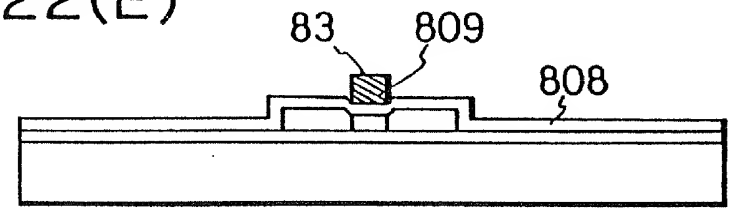


FIG. 22(F)

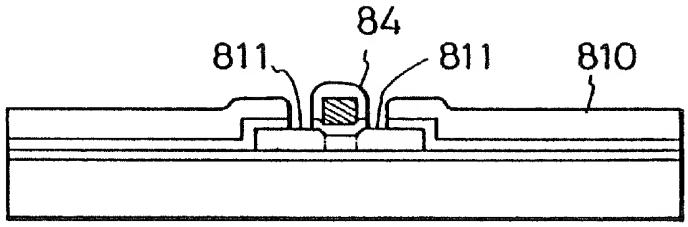


FIG. 22(G)

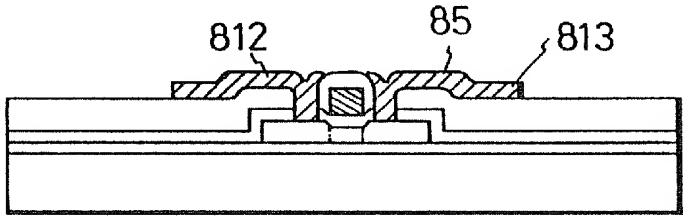


FIG. 22(H)

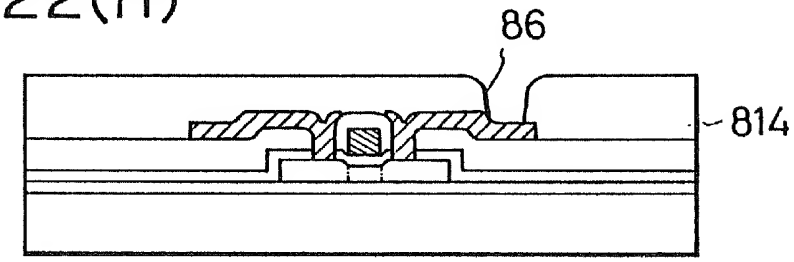


FIG. 22(I)

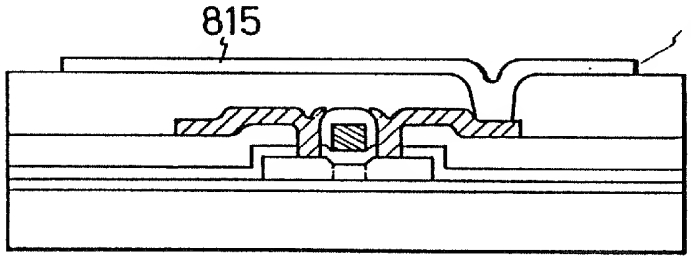


FIG. 23(A)

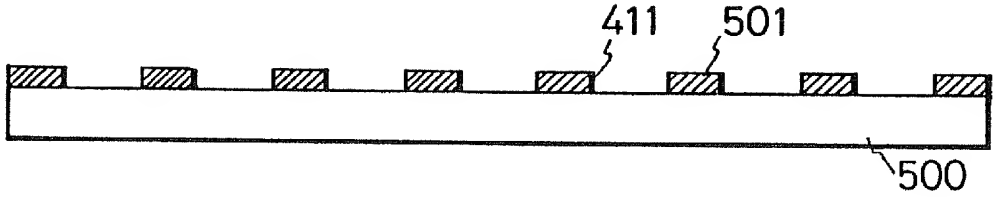


FIG. 23(B)

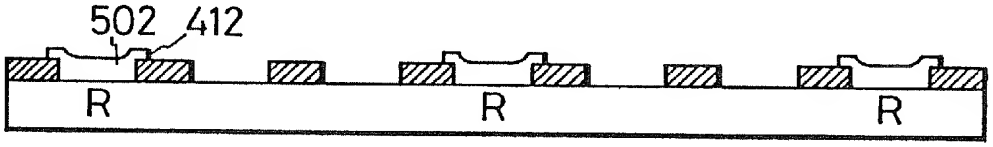


FIG. 23(C)

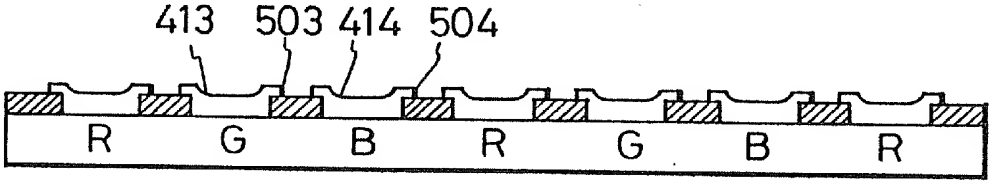


FIG. 23(D)

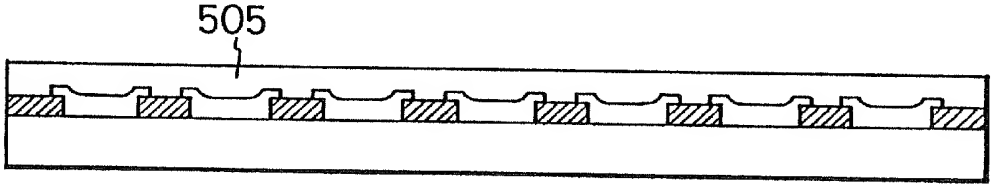


FIG. 23(E)

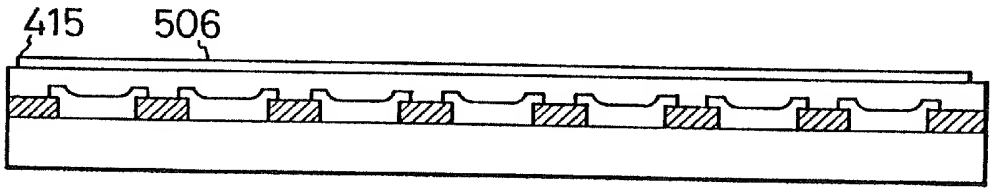


FIG. 24

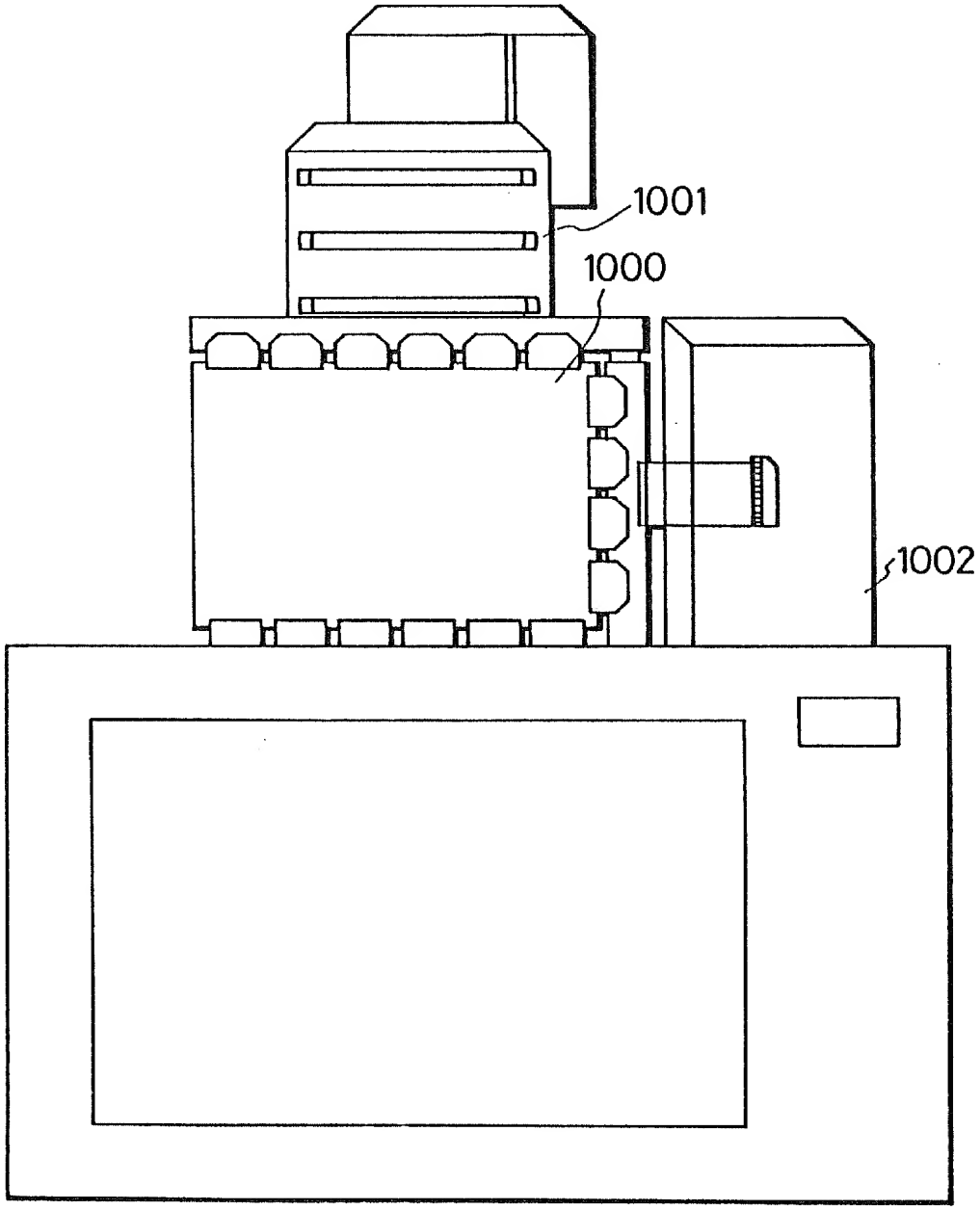


FIG. 25

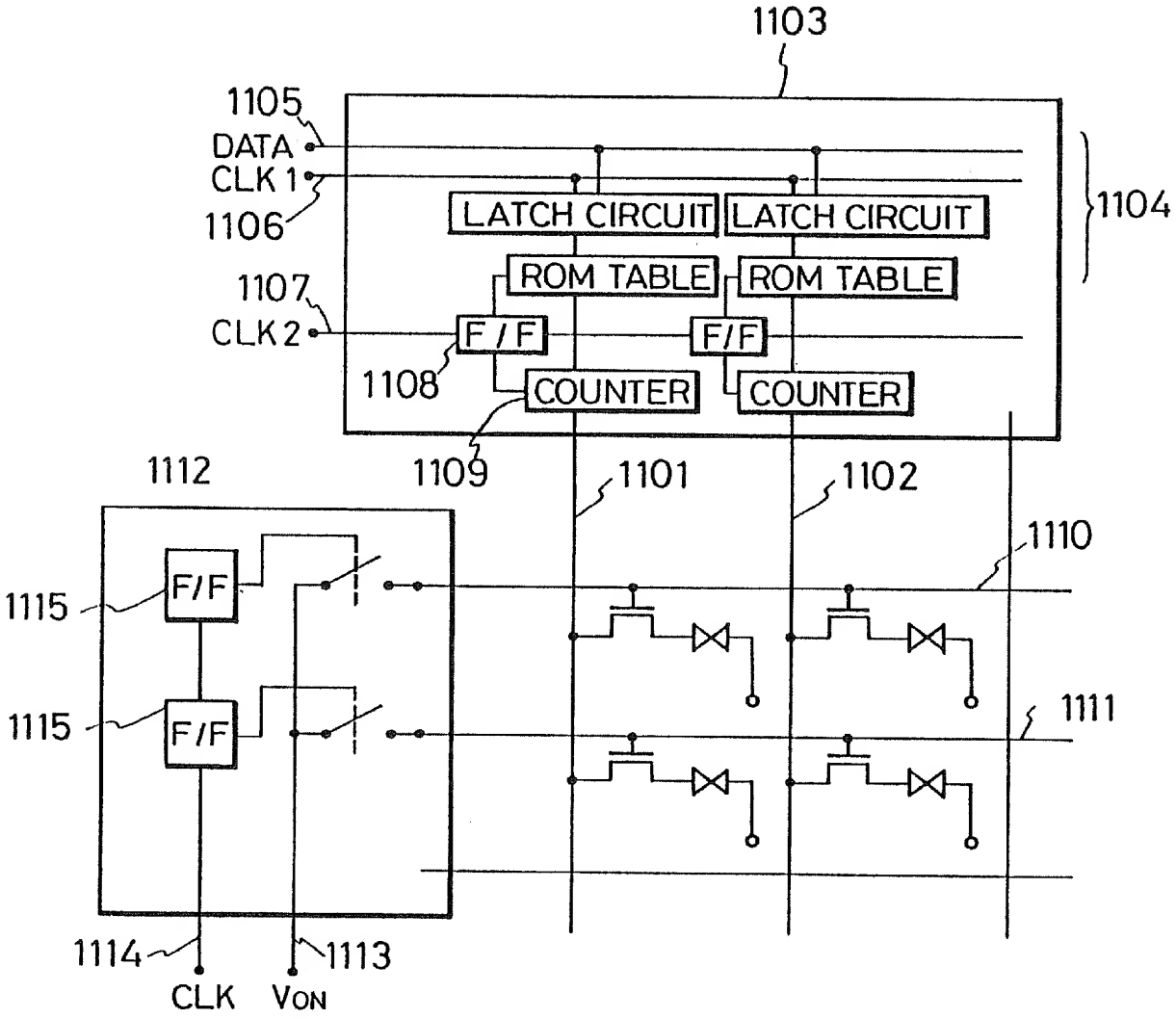

1103
1105
DATA
CLK1
1106
LATCH CIRCUIT
LATCH CIRCUIT
1104
ROM TABLE
ROM TABLE
1107
CLK2
F/F
F/F
1108
COUNTER
COUNTER
1109
1112
1101
1102
1110
1115
F/F
1115
F/F
1111
1114
1113
CLK
VON

FIG. 26(A)

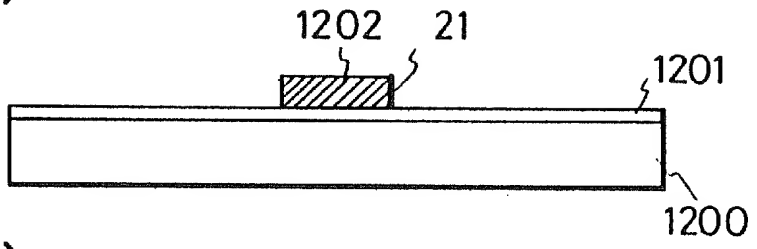


FIG. 26(B)

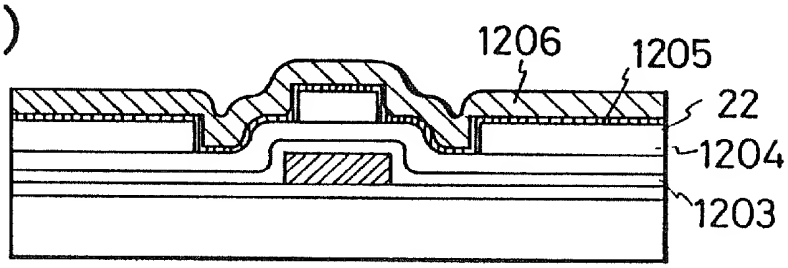


FIG. 26(C)

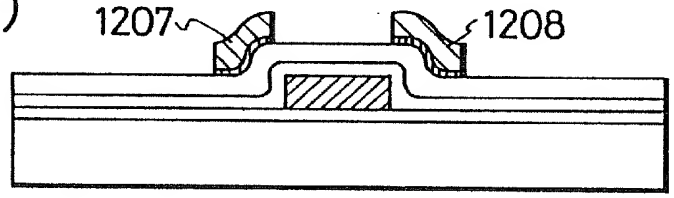


FIG. 26(D)

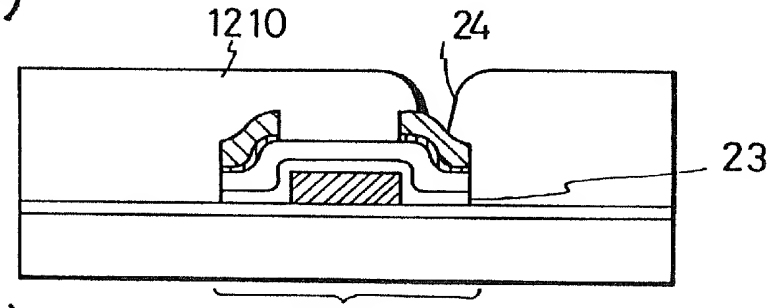


FIG. 26(E)

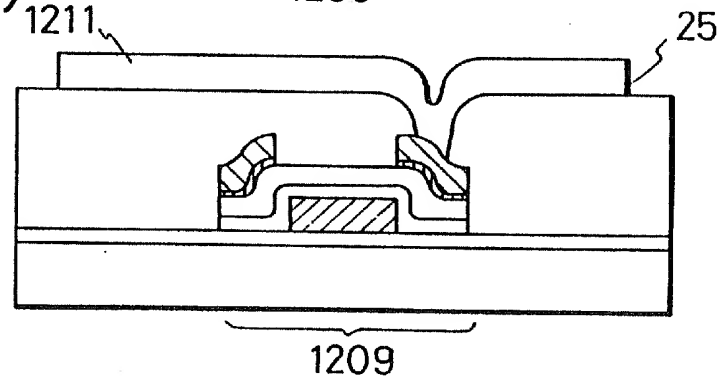


FIG. 27(A)

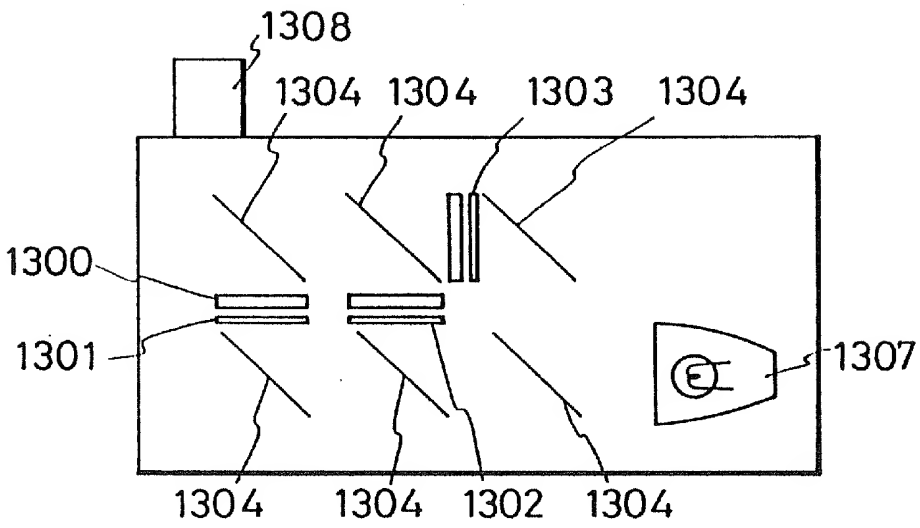


FIG. 27(B)

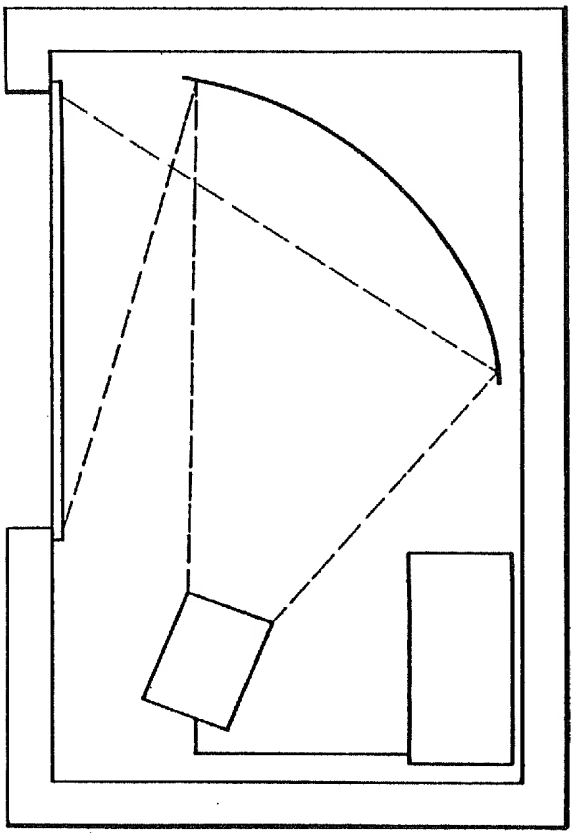


FIG. 28(A)

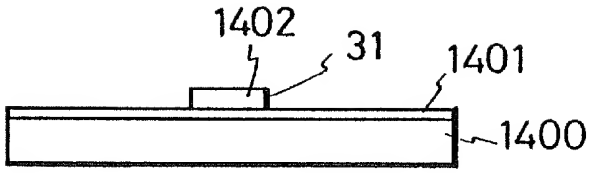


FIG. 28(B)

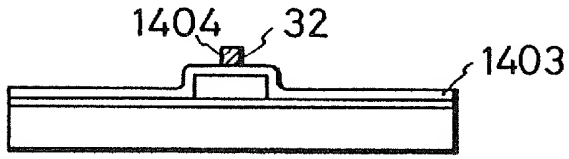


FIG. 28(C)

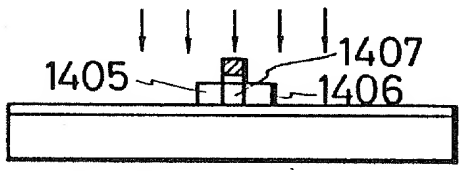


FIG. 28(D)

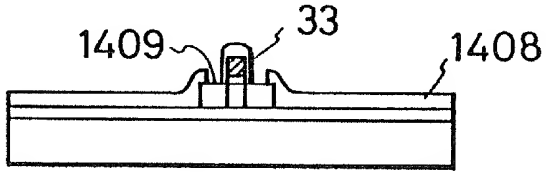


FIG. 28(E)

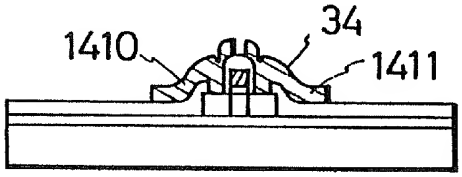


FIG. 28(F)

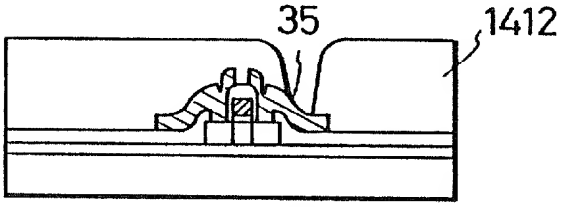


FIG. 28(G)

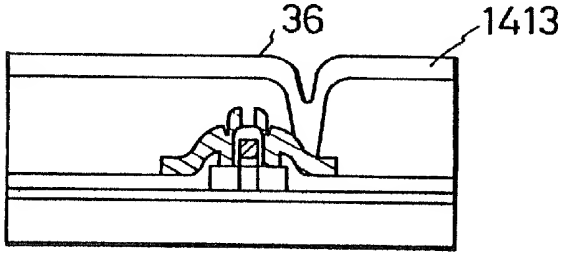


FIG. 29

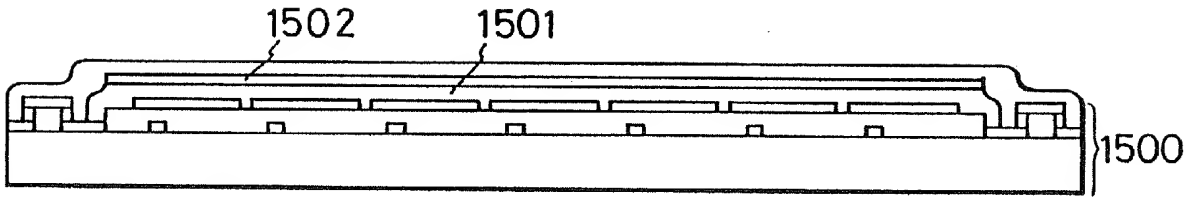


FIG. 30(A)

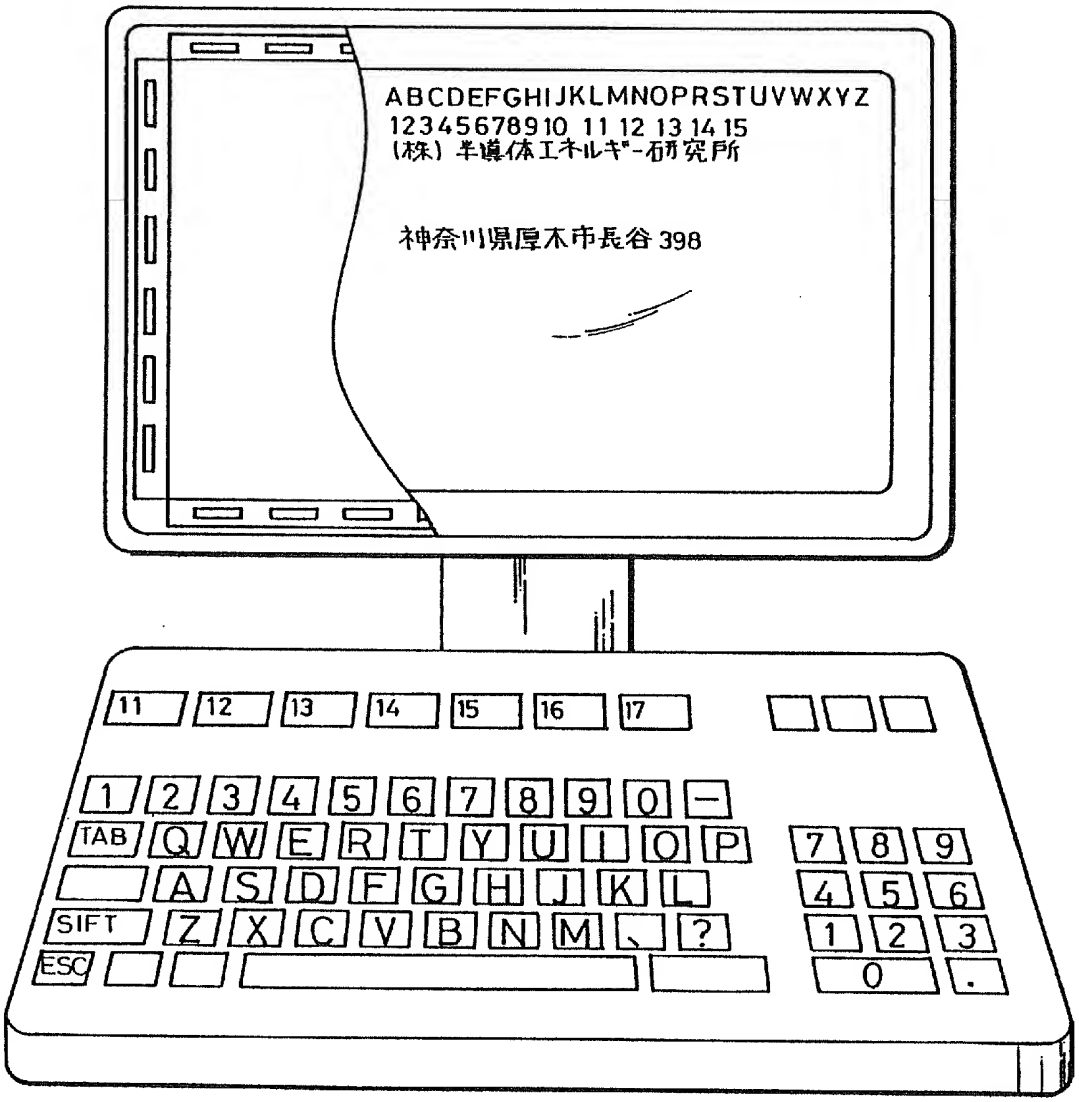


FIG. 30(B)

FIG. 31

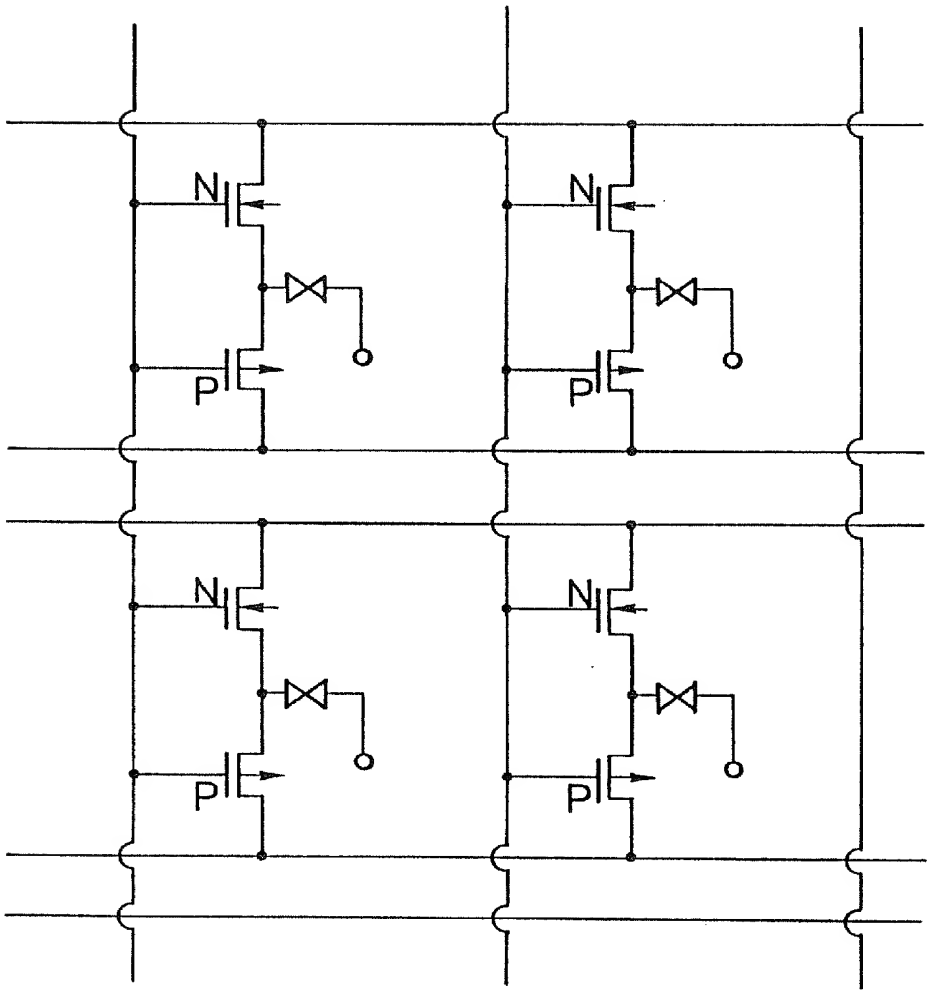


FIG. 32A

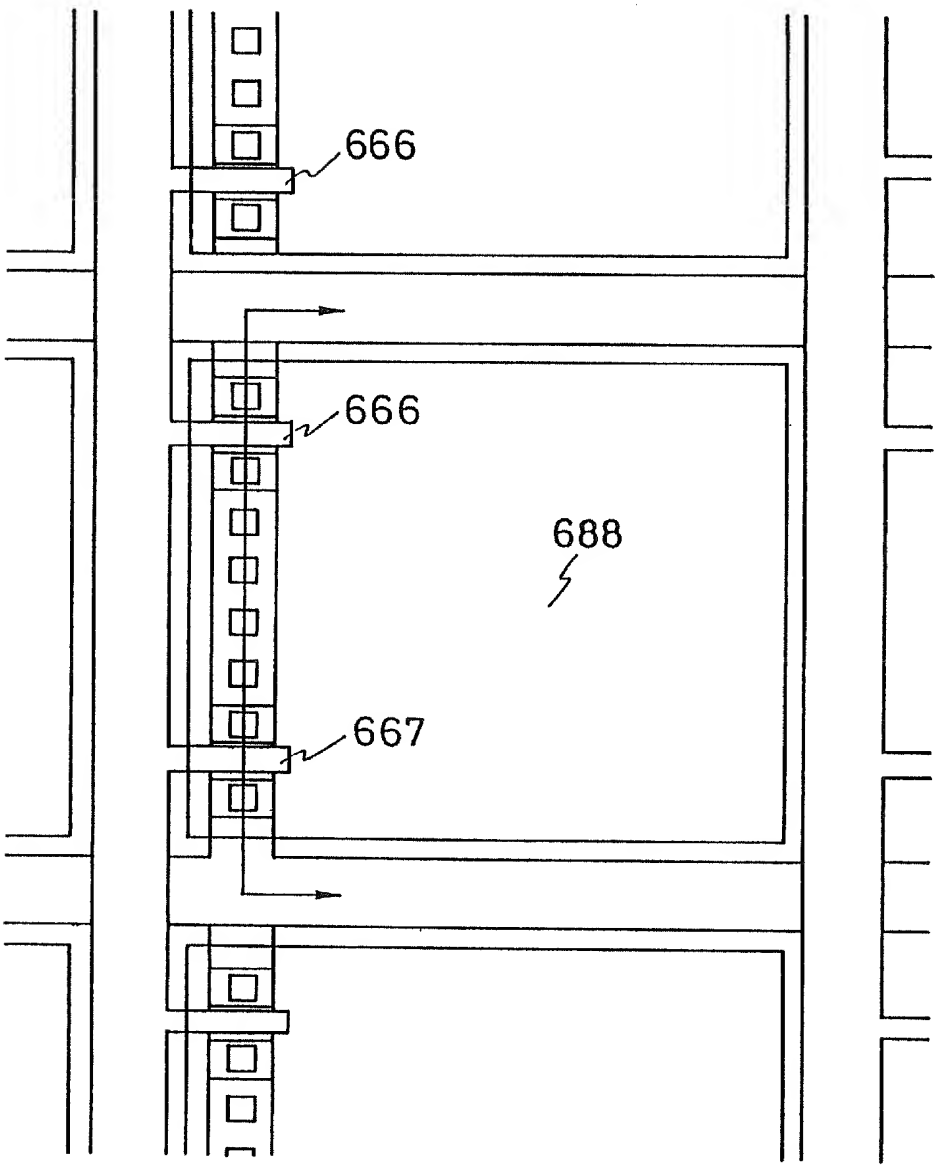


FIG. 32B

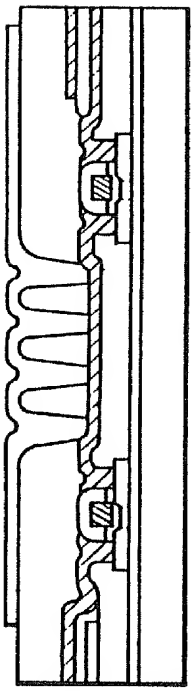


FIG. 33(A)

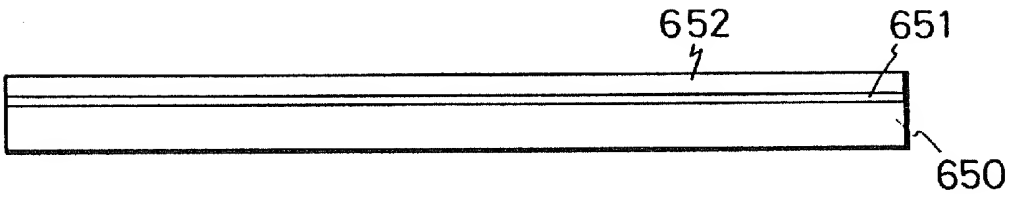


FIG. 33(B)

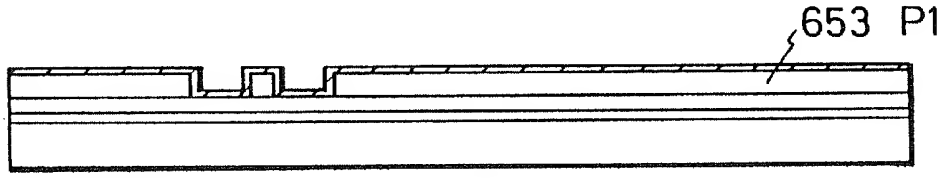


FIG. 33(C)

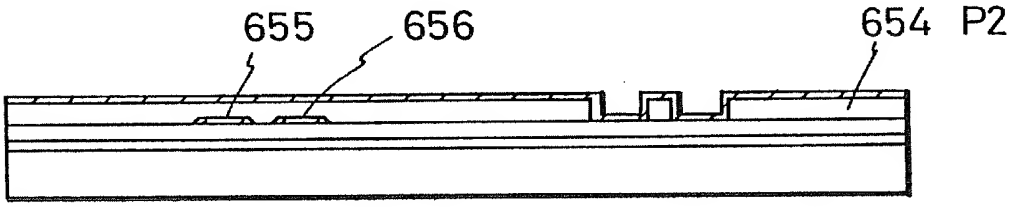


FIG. 33(D)

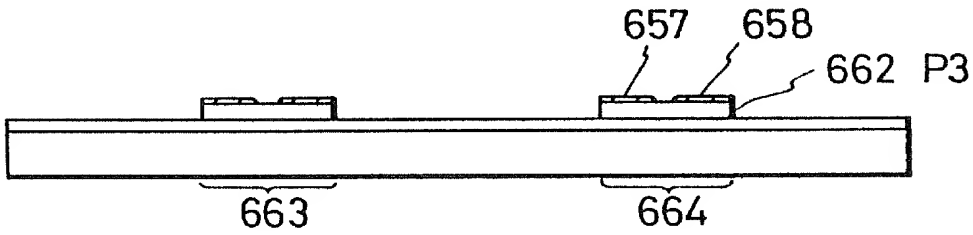


FIG. 33(E)

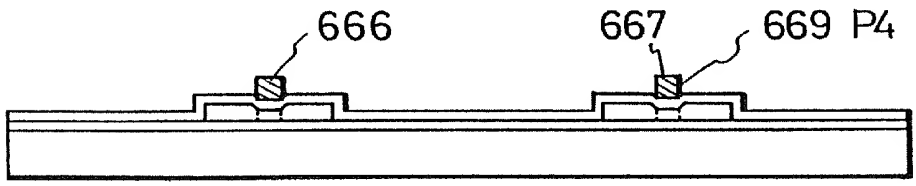


FIG. 33(F)

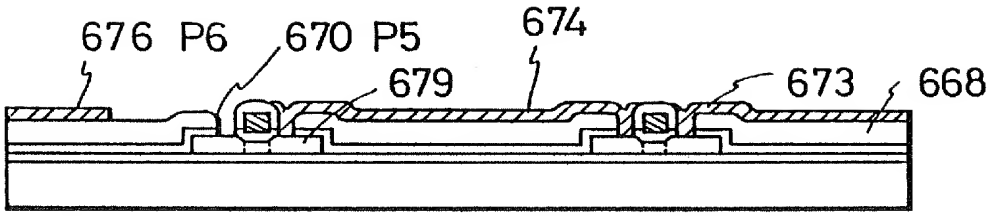


FIG. 33(G)

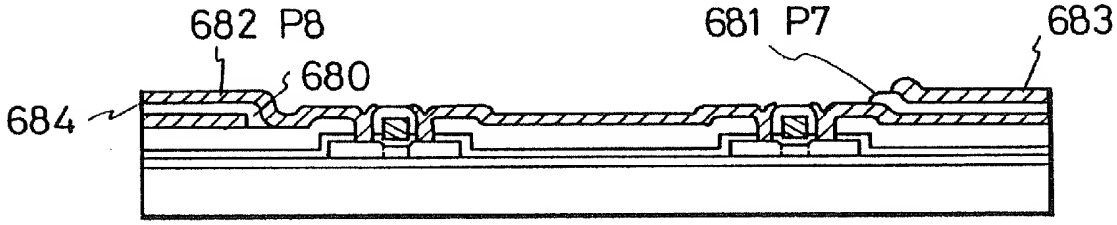


FIG. 33(H)

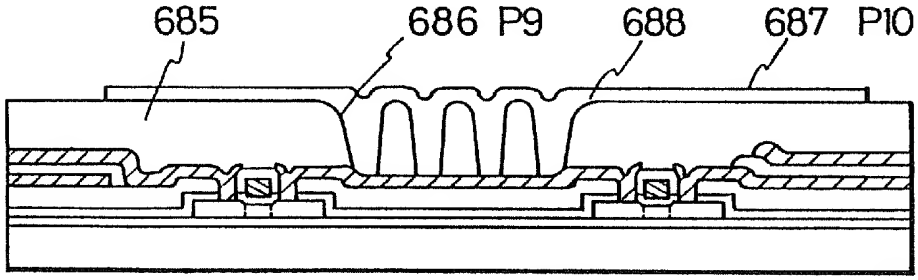
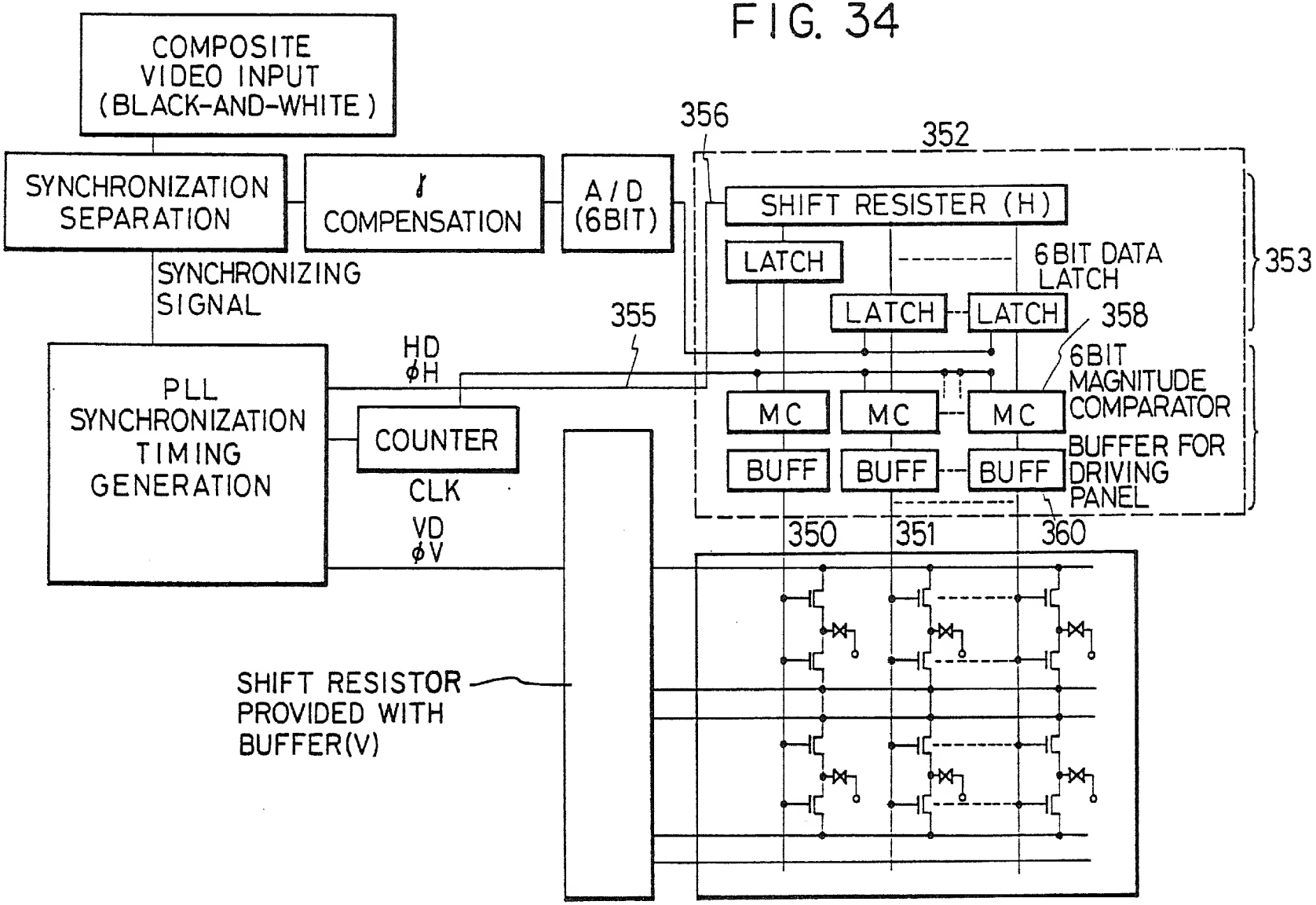


FIG. 34


COMPOSITE VIDEO INPUT (BLACK-AND-WHITE)
SYNCHRONIZATION SEPARATION
γ COMPENSATION
A/D (6BIT)
SYNCHRONIZING SIGNAL
PLL SYNCHRONIZATION TIMING GENERATION
HD φH
COUNTER
CLK
VD φV
SHIFT RESISTOR PROVIDED WITH BUFFER(V)
356
352
SHIFT RESISTER (H)
LATCH
6BIT DATA LATCH
353
LATCH
LATCH
358
355
6BIT MAGNITUDE COMPARATOR
MC
MC
MC
BUFF
BUFF
BUFF
BUFFER FOR DRIVING PANEL
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351
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FIG. 35(A)

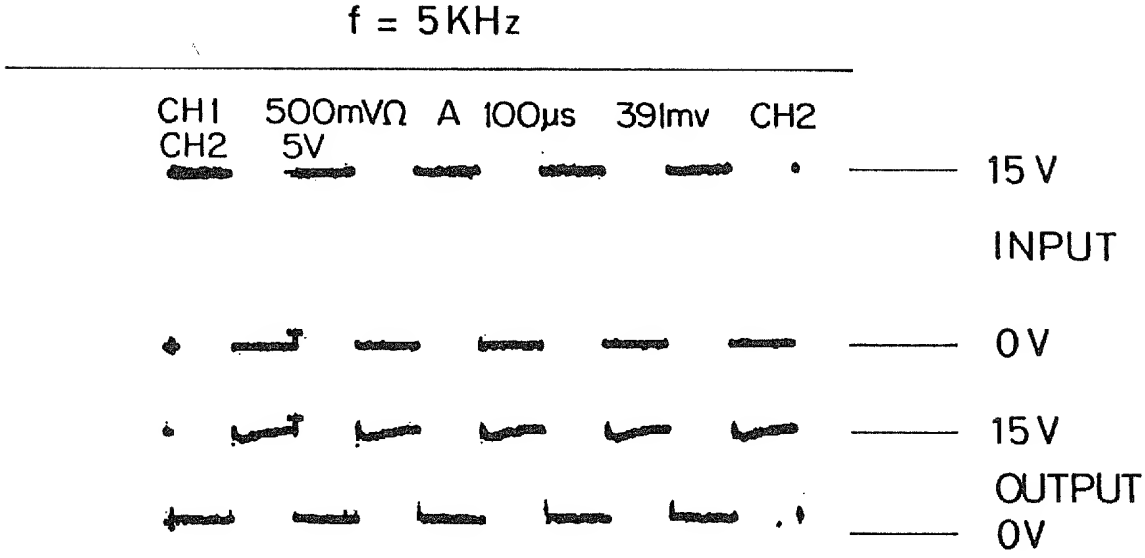


FIG. 35(B)

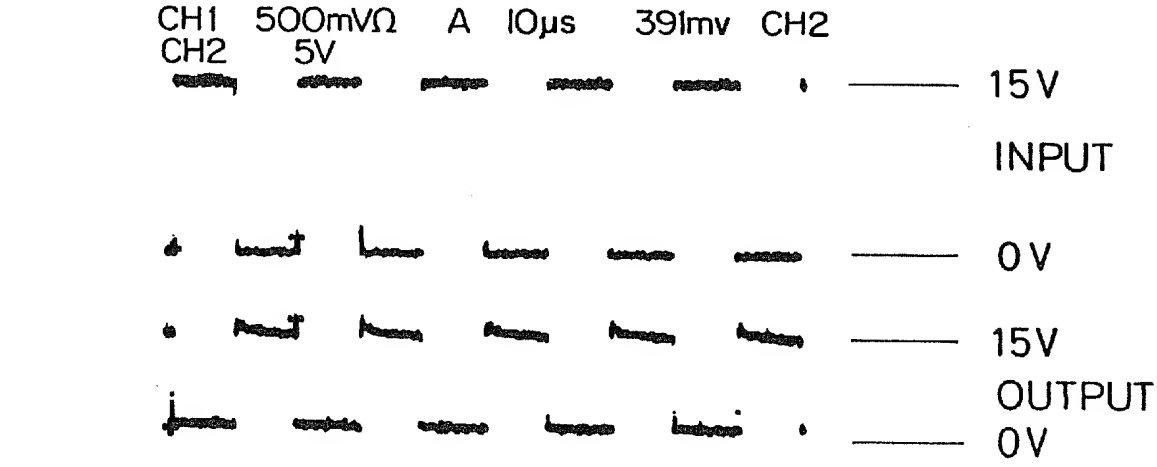


FIG. 35(C)

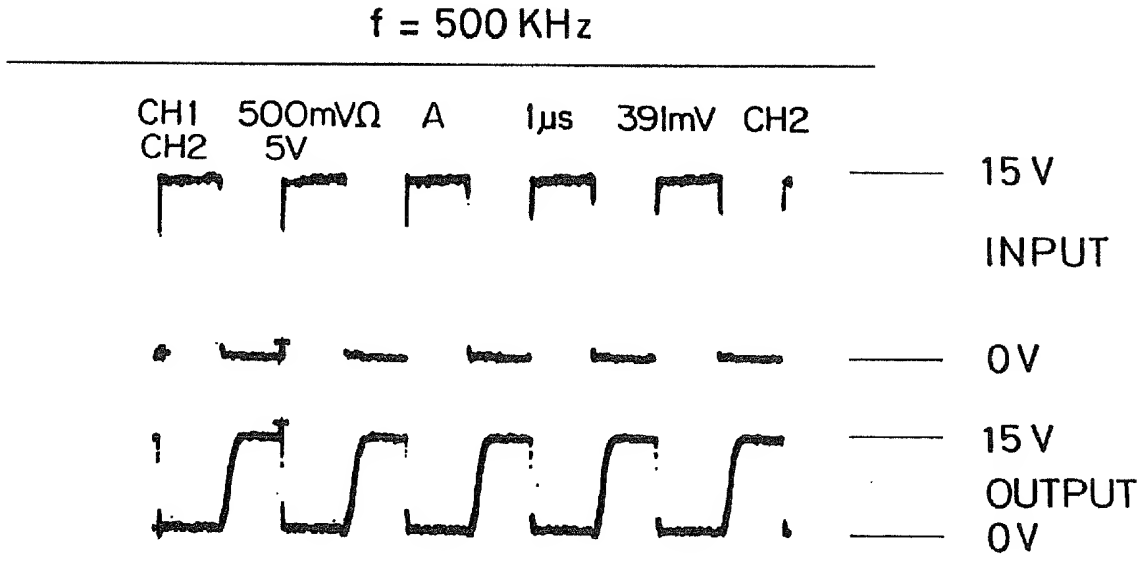


FIG. 35(D)

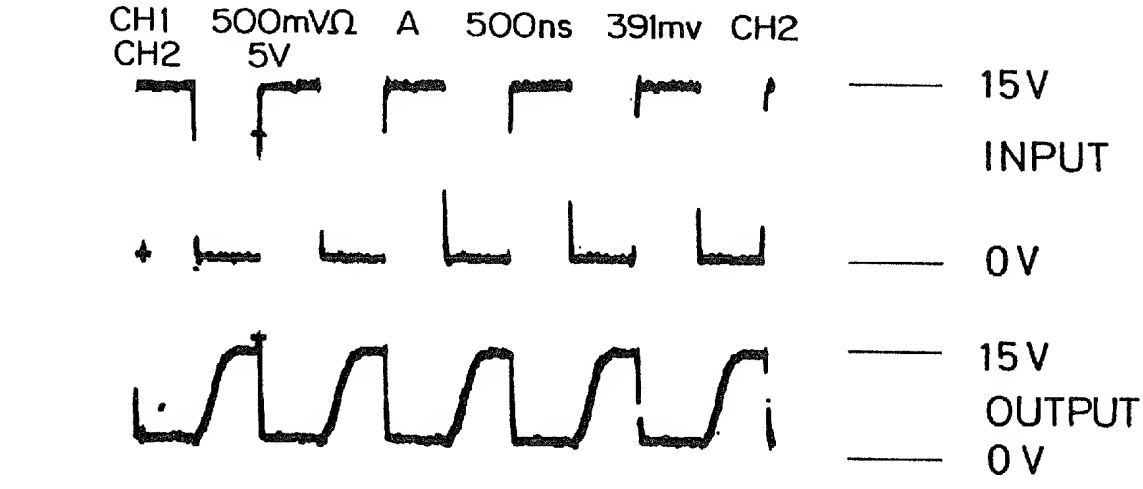


FIG. 36(A)

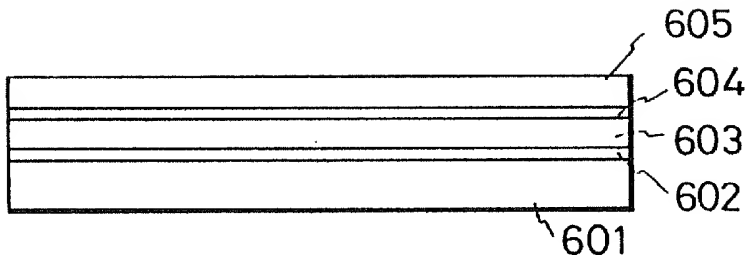


FIG. 36(B)

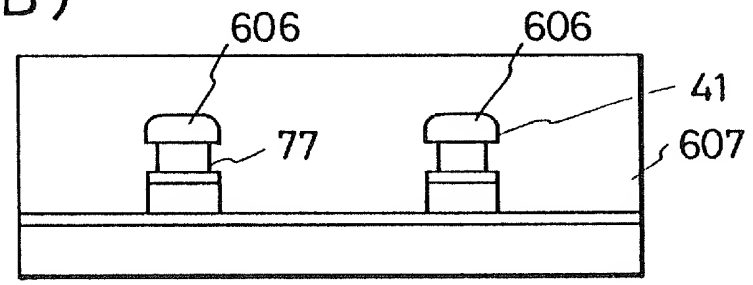


FIG. 36(C)

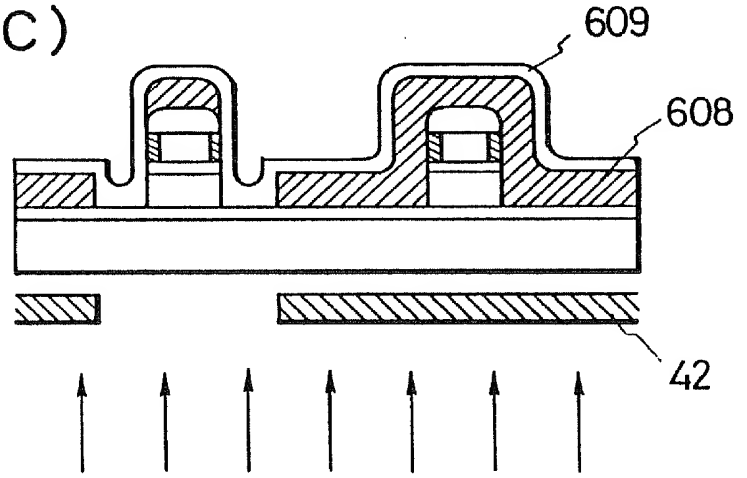


FIG. 36(D)

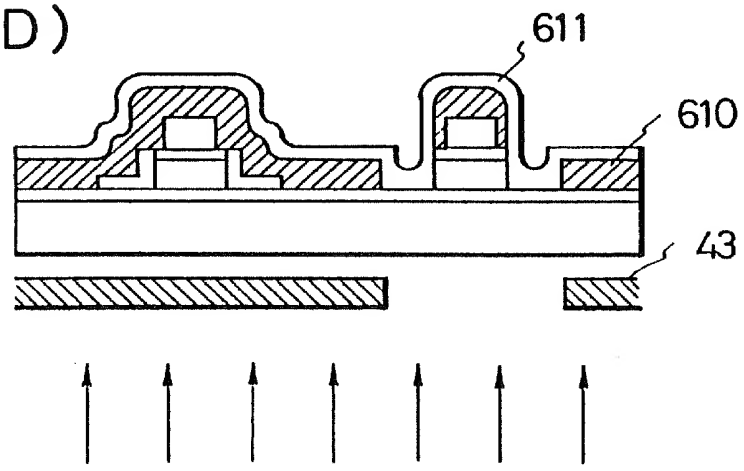


FIG. 36(E)

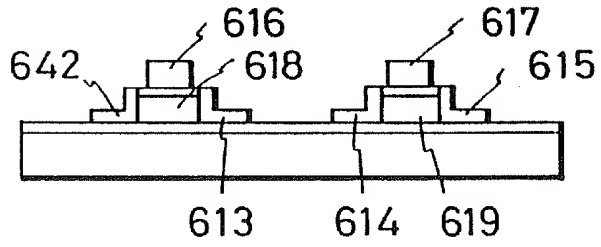


FIG. 36(F)

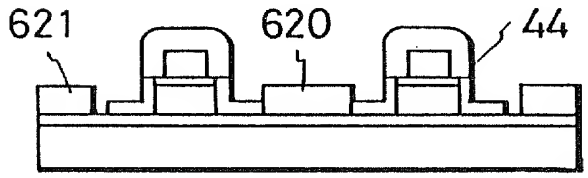


FIG. 36(G)

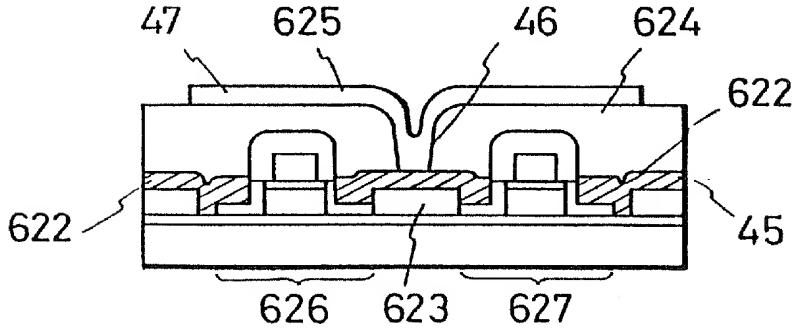


FIG. 37

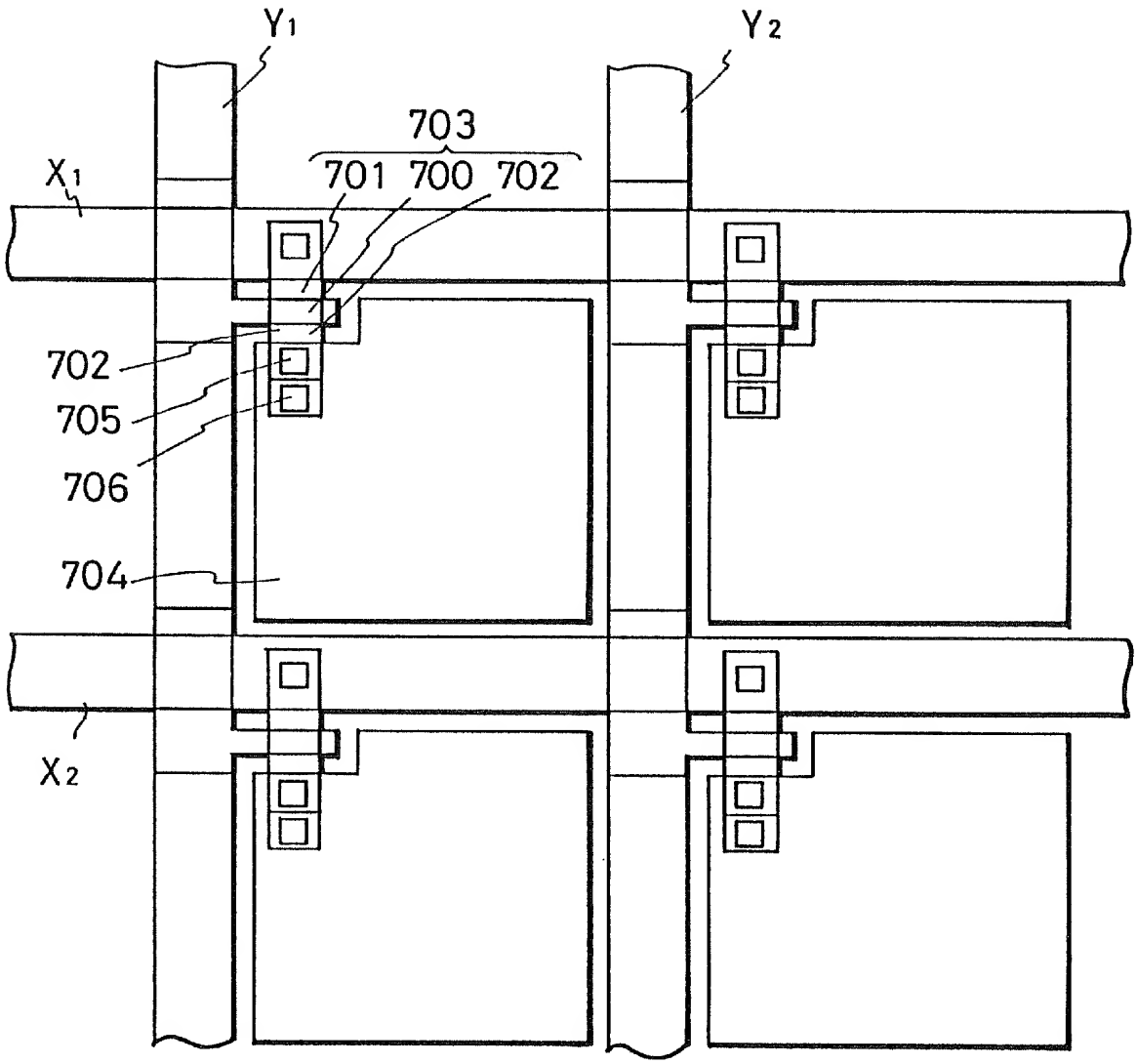
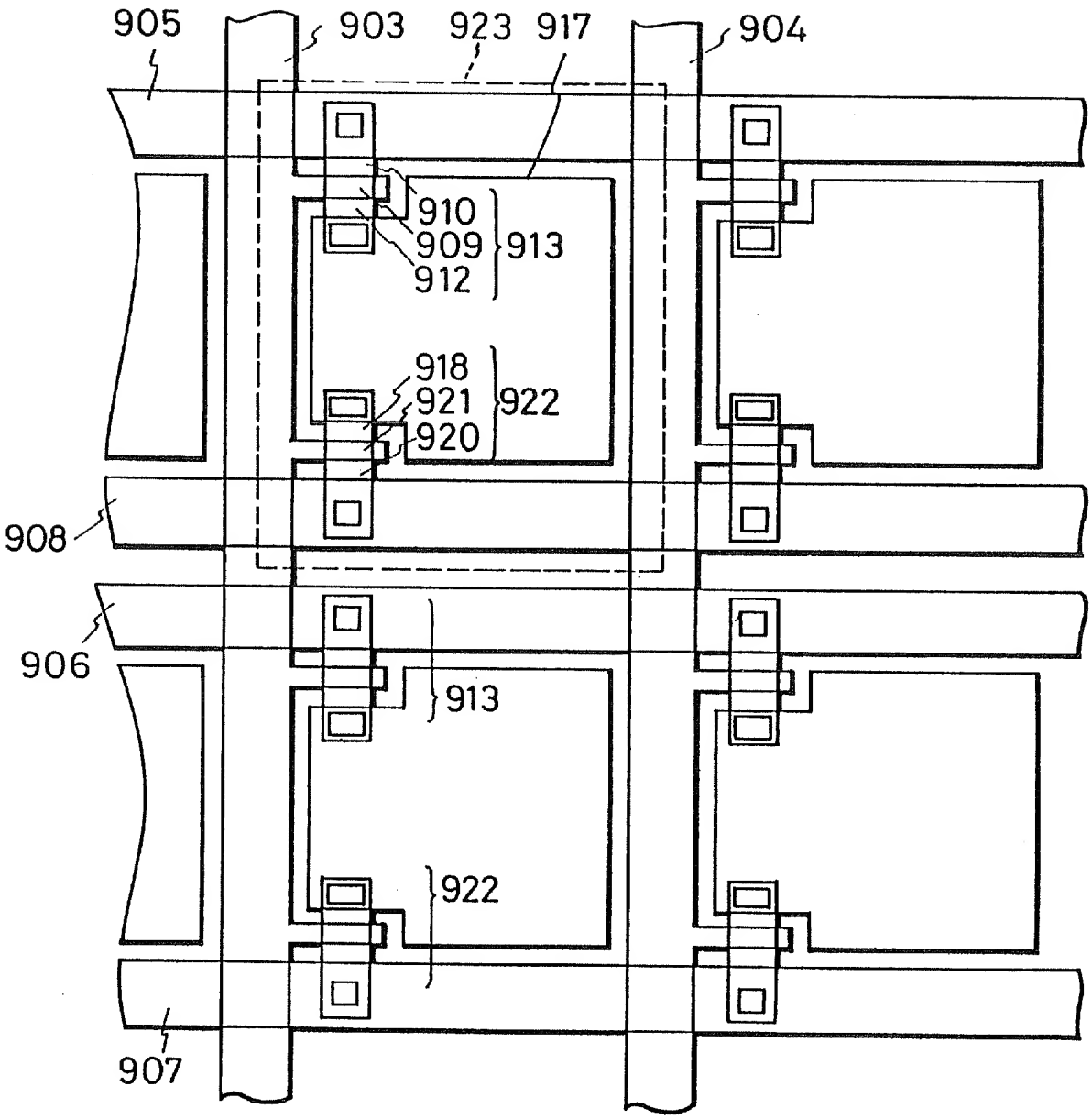


FIG. 38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